Price: $3.50

SDS 925/930/9300 INPUT/OUTPUT INTERFACE DESIGN MANUAL

SDS 900561A

December 1965

SDS

SCIENTIFIC DATA SYSTEMS • 1649 Seventeenth Street • Santa Monica, Calif. • (213) 871-0960

PREFACE

This manual describes the Input/Output System available with the SDS 925/930/9300 Computers with special emphasis placed on the available interface signals and connections. The interface described represents the junction between the Input/Output communication channels and the external equipment. In the case of System Priority Interrupts it describes the junction requirements between external interrupt input signals and the Priority Interrupt Chassis. Detailed descriptions of each available interface connection is stressed to facilitate the efficient design or implementation of the coupling electronics required to connect external units to the computer; therefore, the reader should be familiar with the following publications pertinent to his specific application.

SDS 925 Reference Manual	900099A
SDS 925 Theory of Operation Manual	900633
SDS 930 Reference Manual	900064B
SDS 930 Theory of Operation Manual	900066
SDS 9300 Reference Manual	900050C
SDS 9300 Theory of Operation Manual	900570
Models 93200/93202 TMCC	900685
Model 91602 Data Multiplex Channel - DMC	900828
Model 91500 Memory Interface Connection	900808

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SECTION I INPUT/OUTPUT SYSTEMS

GENERAL DESCRIPTION

The standard I/O system provided with all SDS 925/930/9300 Computers allows operations with all standard SDS peripheral equipment as well as with special purpose devices. Alternate I/O system options are available which are of particular use for systems handling multiple sources of data and for systems requiring very high data acquisition rates.

Two separate paths along which I/O data can flow to and from memory are provided for the SDS 925/930/9300 Computers. Figure 1-1 shows input/output memory paths and systems configuration. The first path is the normal path that exists between memory and the central processor; the second path exists between memory and the I/O control units via a Multiple Access to Memory unit (MAM). Advantages of the multiple access to memory feature are: I/O memory accessing without loss of computation time; higher data transfer rates; and program simplification. Although all I/O channels available with the multiple access to memory option are available to the SDS 925, this computer treats all input and output operations on a priority time multiplexed basis only since the SDS 925 can have no more than one memory bank.

The first path of data flow between memory and central processor uses the following methods of I/O information transfer:

a. Time Multiplexed Communication Channels (TMCC)

b. Parallel Input (PIN)

c. Parallel Output (POT)

d. Single-Bit Input/Output

The second path of data flow between memory and I/O control units and devices uses the following methods of transfer:

a. Data Multiplexing System (DMS)

b. Direct Access Communication Manuals (DACC)

c. Memory Interface Connection (MIC)

All second path to memory systems communicate with memory through a Multiple Access to Memory unit (MAM). Two or more separate memory banks are a prerequisite for taking full advantage of the multiple access to memory option.

TIME-MULTIPLEXED COMMUNICATION CHANNEL (TMCC)

The basic 925/930/9300 configuration includes one TMCC for 6-bit character input/output. This TMCC is referred to as the W channel in the 925/930 and as the A channel in the 9300. The TMCC is capable of controlling I/O devices such as typewriter, paper tape, card, magnetic tape, and line printers on a time multiplexed basis. A computer may have from one to four TMCC's connected to it. Additional channels are designated Y (B on 9300), C, and D. The basic model number is 93200. Model numbers for additional channels and optional features are listed in table 1-1. Any 6-bit TMCC can be expanded to 12 bits by adding the Model 93201 option or to 24 bits by addition of the Model 93202 option. With the 12- and/or 24-bit options character size is controlled by the external device. The 24-bit buffer can handle either 6, 12, or 24 bit characters according to device requirements.

Table 1-1. TMCC Models

Model	Description	Used on Channel
93200	6-bit characters, without interlace, single channel	W(A), C
91210	Interlace option for 93200	
93201	12-bit character extension option for 93200	
93202	24-bit character extension option for 93200	
93221	6-bit characters, without interlace, two channels	W(A) plus Y(B) or C plus D
91210	Interlace option for either channel of 93221	
93201	12-bit character extension option for either channel of 93221	
93202	24-bit character extension option for either channel of 93221	

The memory interlace feature may be added to any TMCC by adding the Model 91210 Memory Interlace Control unit. This optional feature is useful for input/output of large blocks of data at high transfer rates. The memory interlace automatically controls the transfer of data words for its associated channel buffer by maintaining a current memory address and word count during input/output operations.

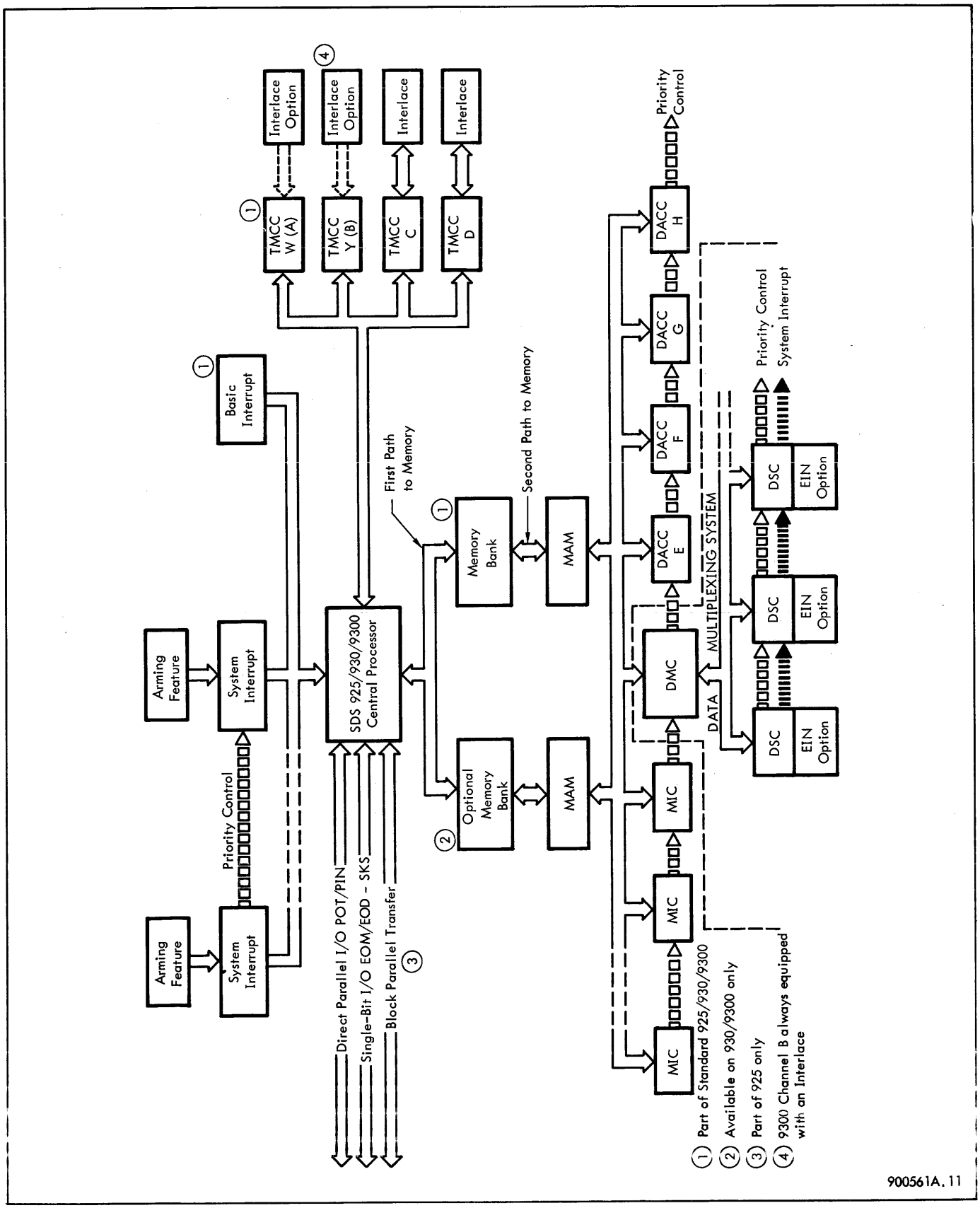


Figure 1-1. 925/930/9300 General Computer Configuration

The interlace also controls terminal functions and provides end-of-record and zero word count interrupts.

Channels C and D (and B on the 9300) must always have interlace installed since no computer instructions exist in the 9300 to allow use of these channels without interlace. Any TMCC operating with interlace has priority over the central processor for memory access with channel priority in the order: Channels D, C, Y(B), W(A).

The maximum data transfer rate of a TMCC is one word every two memory cycles or 280,000 words per second.

POT,PIN INSTRUCTIONS

The 925/930/9300 Computers include two instructions, parallel output and parallel input, which permit the transfer of words between core memory and external equipment without interfering with the operation of other I/O channels. The execution of either the POT or PIN instruction causes a signal to be sent to the external device requesting it to acknowledge when it is ready to receive or transmit the data word. After the request signal is sent, the computer suspends operations until the acknowledge signal is received. The maximum data transfer rate for PIN operations is 114,000 words per second (five cycles for each word transfer). The maximum data transfer rate for POT operations is 143,000 words per second (four cycles for each word transfer).

The Block POT and Block PIN (BPO/BPI) operations which are unique to the SDS 925 transfer words at a maximum rate of 570,000 words per second (one cycle for each word transfer).

SINGLE-BIT INPUT/OUTPUT

The two instructions, Energize Output M (EOM) and Skip If Signal Not Set (SKS) when operating in the system mode are used to provide single-bit input/output transmission. Execution of an EOM operating in the system mode causes a signal to be transmitted to one of a possible 8,192 signal destinations. The maximum signal transfer rate is 570,000 pulses per second. Execution of an SKS in the special system test mode permits the computer to test the condition of any one of a possible 8,192 input lines. The maximum test rate depends on the condition of the line: 286,000 per second if program does not skip next instruction, or 190,000 per second if program does skip the next instruction.

MULTIPLE ACCESS TO MEMORY

The Multiple Access to Memory feature (MAM) provides the necessary modules on both main frame and memory to permit memories to be accessed via the second memory path. Transfer of one word over this path in either direction requires one memory cycle. If the computer has two or more memory banks, the main frame can communicate with one memory via the first path to one memory while some peripheral device is communicating with the other memory via the second path without interference or loss of computation time.

The Multiple Access to Memory feature (MAM) is required for the attachment of Direct Access Communication Channels (DACC), Data Multiplex Channels (DMC), or Memory Interface Connections (MIC).

DIRECT ACCESS COMMUNICATION CHANNEL (DACC)

The Direct Access Communication Channel, Model 92220, is available for systems requiring high-speed input/output simultaneous with computation. Up to four DACC's may be connected to the core memory through the Multiple Access to Memory (MAM), Model 92990 (Model 92992 for the 925) for each memory module. The four channels are designated E, F, G, and H. Simultaneous access to memory will occur if the channel and computer are addressing separate memory modules. If simultaneous access to the same memory module is required, priority is in the order: MAM, TMCC, Central Processor.

The maximum data transfer rate in the high-speed mode is one word every memory cycle, or approximately 570,000 words per second.

The DACC communicates with external equipment by means of a bidirectional 24-bit register using 6-, 8-, 12-, or 24-bit characters plus a parity bit. Character size is controlled by the external device.

DATA MULTIPLEXING SYSTEM (DMS)

The data multiplex system consists of two basic elements:

a. The Data Multiplex Channel (DMC) for communicating with several data sources/destinations, and for synchronizing I/O operations with memory.

b. One or more Data Subchannels (DSC) for interfacing between peripheral devices or systems and the DMC.

Data Multiplex Channel (DMC)

The data multiplex channel is equipped with an internal interlace feature that allows specified input/output tables in memory to be processed by the addressed peripheral device via the associated subchannel.

Data Subchannels (DSC)

Two standard subchannels are available. Model 91711 DSC-I provides character oriented operations, and Model 91712 DSC-II is full-word (24-bit) oriented. Up to 128 DSCs can be attached to the DMC. Two or more DSCs can be active simultaneously using an internal priority arrangement to determine which subchannel can transmit to the DMC at any given time.

External Interlace (EIN)

An External Interlace Model 91800 can be attached to any DSC. The EIN controls the transmissions of the DSC at a maximum rate of one word per memory cycle. Maximum data transfer rate using internal interlace is 190,000 words per second. With external interlace the maximum transfer rate is increased to 570,000 words per second.

MEMORY INTERFACE CONNECTION (MIC)

The Memory Interface Connection, Model 91500, is available for direct access to core memory under control of external equipment. A prerequisite for MIC is a Multiple Access to Memory (MAM) Model 92990 for each memory module. The 925 Computer requires the Multiple Access to Memory (Model 92992). The external device must provide signals to the MIC indicating when an I/O operation is to take place, it must specify the memory address, and must indicate whether the function is an input or an output. The MIC checks parity on inputs and generates parity on outputs. Data transfer is in the form of 24-bit words plus odd parity.

The maximum data transfer rate is 570,000 words per second.

PRIORITY INTERRUPT

The 925/930/9300 Computers are capable of program sequence interruption by signals generated by communication channels, special features, and external equipment, on a priority basis. Each 925/930/9300 includes a basic interrupt unit that provides two interrupts (four for 9300) with 22 more available (20 more for 9300) for use with optional I/O channels and special features. Up to 896 system priority interrupts for general purpose use are available for external systems by adding Model 93280 interrupt control units. Each Model 93280 can control up to 32 priority interrupts. The Model 93280 does not include the interrupts. However, interrupts may be added to the Model 93280 by connecting a Model 93290 priority interrupt. Each Model 93290 contains two levels of priority interrupt; thus 16 Model 93290's (32 levels of interrupt) can be added to each interrupt control unit.

An arming feature may be added to the interrupt control unit by adding a Model 92280 arming option to provide arming for the first 16 levels of interrupt on a Model 93280. Arming for the second 16 levels of interrupts can be added by adding a Model 92290 arming option to the Model 92280.

SECTION II INPUT/OUTPUT INSTRUCTIONS

GENERAL

Five instructions control input/output operations of the 925/930/9300 Computers. These are:

a. Energize Output M (EOM)

b. Energize Output to Direct Access Channels (EOD)

c. Parallel Input (POT)

d. Parallel Input (PIN)

e. Skip If Signal Not Set (SKS)

In addition to the five instructions above the SDS 925 provides for a block transfer variation of the POT and PIN operations, BPO and BPI. In this manual emphasis is placed on interface information and the reader should refer to the 925, 930, or 9300 reference manual for a detailed description of each instruction.

ENERGIZE OUTPUT M (EOM)

The EOM instruction is used primarily to control input/output through all channels except the DACC. This instruction operates in four basic modes that are program selectable by the setting of two bits (C10, C11) within the EOM instruction format:

C10	C11	Function
0	0	Buffer Control
0	1	Input/Output Control
1	0	Internal Control
1	1	System Control

One computer cycle (1.75 μsec) is required to execute an EOM instruction in any mode. During the execution of the EOM instruction the control register (C register) of the computer is held stable. At that time this 24-bit register (C0-C23) contains the EOM instruction word. The output of this register is available to the TMCC and to the external units. If an interrupt occurs during the execution of any EOM in any mode, it will not be acknowledged until the execution of the instruction following the EOM is complete.

Buffer Control EOM

The EOM instruction operating in the buffer control mode prepares the channel and device for data transmissions or other peripheral activities. The channel to be used, the peripheral unit on that channel, the operation to be performed, and the type of character format to be used, are all detailed within the EOM in this mode. The use of BCD or binary data transmission, the allowance or not of a leader (as in paper tape functions), and the direction of operation (in magnetic tape functions) are all detailed to the channel and its connected peripheral unit. Execution of such an EOM connects the specified peripheral unit to the channel. Interlace can also be alerted with EOM in this mode.

Internal Control EOM

The EOM in the internal control mode is used to enable and disable the interrupt system, to prepare the system for the selective arming and disarming of the system interrupt levels, to reset the overflow, and to record exponent overflow. The EOM, internal control mode, does not apply directly to I/O control, and therefore, it does not generate interface signals.

Input/Output Control EOM

The EOM in the input/output mode is used to direct peripheral devices to perform nontransmitting operations such as rewind magnetic tape and upspace the printer. Selection of certain channel operations such as interrupt response and the input/output terminal function desired is made with this EOM. It is also used to alert peripheral devices that a Parallel Input (PIN) or Parallel Output (POT) instruction is to follow. The C register outputs, C18 through C23, must be decoded by the external unit during this instruction to avoid interference with standard device control.

System Control EOM

The EOM in the system control mode can control internal equipment by providing a single-bit output of approximately 1.4 μsec to any addressable connector. The system control mode can be divided into two distinct submodes by gating bit 9 with bits 10 and 11 of the system mode EOM.

C1	C9	C10	C11	
X	0	1	1	EOM System Control (External)
X	1	1	1	EOM System Control (Internal)

The internal system control submode provides control for standard I/O systems such as the DMS, data communications, and display. The external system control submode provides a means of controlling special non-standard I/O equipment or systems. C1 must always be included in the decoding circuitry since the term C1 separates the Data Multiplex System ($\overline{C1}$) from other I/O buffer units (C1).

EOM Interface Signals

Four signals generated by the EOM instruction are available at the TMCC I/O connectors. See figure 2-1. These signals, when true, indicate that the contents of the C register (C0-C23) are to be transferred to external equipment. The four signals are:

a. (Eom)
b. (Buc) (Buffer Control Mode)
c. (Ioc) (I/O Control Mode)
d. (Sys) (System Control Mode)

The signals, (Buc), (Ioc), and (Sys), indicate to the external system which EOM mode is currently being executed.

The Eom signal is generated by all EOM instructions, and is true during periods T7 - Tr (1.4 µsec). The Eom pulse is also generated during the FILL operation. The Eom signal is inhibited during the second EOM instruction of the interlace loading sequence and during time-share operations.

The signals, (Buc) and (Ioc) are derived from the EOM instruction according to configuration of bits C1, C10, and C11.

	TMCC	
Signal	W(A) Y(B)	C, D
(Buc)	$\overline{C1}$ $\overline{C10}$ $\overline{C11}$	C1 $\overline{C10}$ $\overline{C11}$
(Ioc)	$\overline{C1}$ $\overline{C10}$ C11	C1 $\overline{C10}$ C11

The terms C17 and $\overline{C17}$ must be used by the external system to distinguish between TMCC-W(A) and TMC-Y(B), and, similarly, between TMCC-C and TMCC-D.

$$\overline{C17} = \text{TMCC-W(A)} \quad \text{or} \quad \text{TMCC-C}$$

$$C17 = \text{TMCC-Y(B)} \quad \text{or} \quad \text{TMCC-D}$$

The (Sys) signal is derived from the EOM instruction (external system submode) according to bits C9, C10 and C11.

$$(\text{Sys}) = \overline{C9}\ C10\ C11$$

If the contents of the C register (C0, C1, C2, C12-C23) are decoded during the (Sys) signal, up to 32,768 single-bit outputs can be obtained.

ENERGIZE OUTPUT TO DIRECT ACCESS CHANNELS (EOD)

The EOD instruction is used to control input/output through the DACC. This instruction is similar to the EOM instruction and performs analogous functions for the direct access channels E, F, G, and H.

EOD Interface Signals

Four signals generated by the EOD instruction are available at the DACC I/O connectors. See figure 2-2. These signals, when true, indicate that the contents of the C register

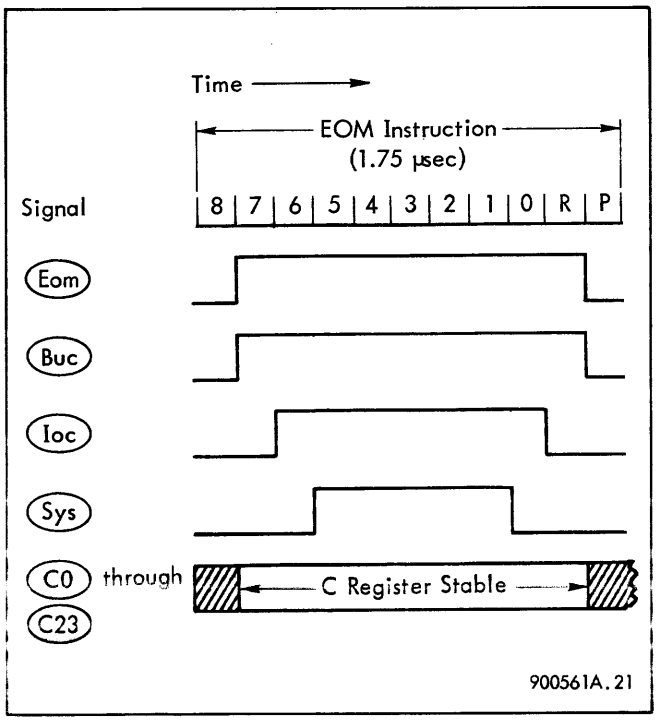


Figure 2-1. Signals Generated by EOM Instructions

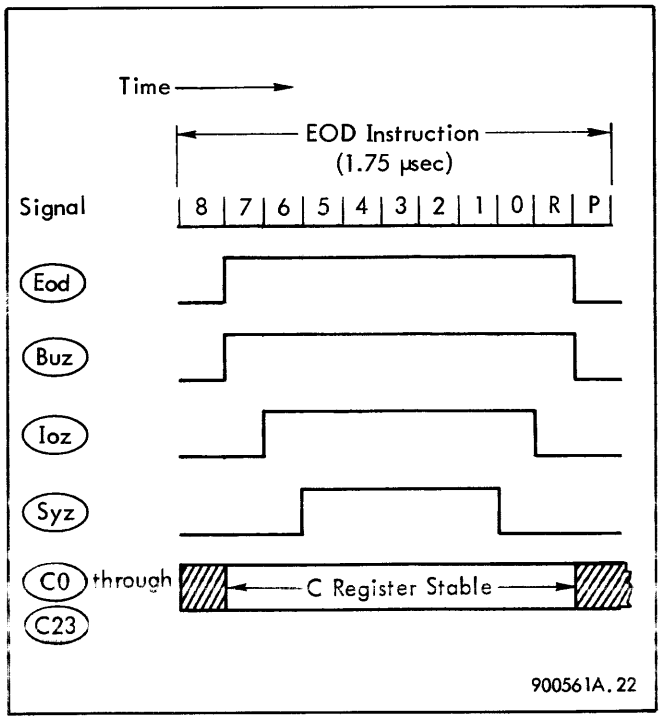


Figure 2-2. Signals Generated by EOD Instruction

(C0-C23) are to be transferred to external equipment. These signals are:

a. (Eod)
b. (Buz) (Buffer Control Mode)
c. (Ioz) (I/O Control Mode)
d. (Syz) (System Control Mode)

The signals, (Buz), (Ioz), and (Syz), indicate to the external system which EOD mode is currently being executed.

Eod is generated by all EOD instructions and is true during periods T7 - Tr (1.4 μsec). This Eod pulse is inhibited during time-share operations and during the interlace loading sequence.

The (Buz) and (Ioz) signals are derived from the EOD instruction according to the configuration of bits C1, C10, C11, and C17.

DACC

Signal	E				F			
(Buz)	$\overline{C1}$	$\overline{C17}$	$\overline{C10}$	$\overline{C11}$	$\overline{C1}$	C17	$\overline{C10}$	$\overline{C11}$
(Ioz)	$\overline{C1}$	$\overline{C17}$	$\overline{C10}$	C11	$\overline{C1}$	C17	$\overline{C10}$	C11
	G				H			
(Buz)	C1	$\overline{C17}$	$\overline{C10}$	$\overline{C11}$	C1	C17	$\overline{C10}$	$\overline{C11}$
(Ioz)	C1	$\overline{C17}$	$\overline{C10}$	C11	C1	C17	$\overline{C10}$	C11

Because C17 and $\overline{C17}$ are included in the (Buz) and (Ioz) terms, external recognition of C17 and $\overline{C17}$ is not required.

(Ioz) is inhibited during the interlace loading sequence.

(Syz) signal is derived from the EOD instruction according to bits C9, C10, and C11.

$$(Syz) = \overline{C9}\ C10\ C11$$

PARALLEL OUTPUT (POT)

The POT instruction provides a means of direct parallel transfer of up to 24 bits from memory to an I/O channel or external device via the C register of the processor. Each word transfer is under direct program control. The POT instruction must be preceded by an EOM instruction to select the desired device. During a POT instruction, the computer accesses the word to be transferred from a location of memory determined by the effective address of the instruction. The computer then proceeds to a wait phase and holds the word to be transferred in the C register.

The wait phase consists of an integral number of computer cycles (1.75 μsec each). During the wait phase, the C register output lines C0-C23 are stable and contain the 24-bit word to be transferred to the external device. Upon receipt of a ready signal from the external device which is to receive the data, the computer exits from the wait phase and continues computation. (The computer will remain in the wait phase, thereby suspending computation, until it is released by the ready signal from the external device). If the device was ready before the computer entered the wait phase, the computer would spend only one cycle in the wait phase and then resume computation. Thus all POT instructions spend at least one computer cycle in a wait phase. The POT instruction requires 2 + n cycles, [(3.5 μsec) + n (1.75 μsec)] where n = number of wait phases for execution.

POT Interface Signals

The following signals are available on POT connectors provided with each DACC and TMCC. See figure 2-3. The ready signal supplied by the external device is designated ($\overline{Rt}$). This signal, when low (0v) indicates that the unit is ready, and when high (+8v) that the unit is not ready. The status of this ready signal is tested once every machine cycle during the wait phase. (The actual sampling time is T7-T3). The ready signal must be at ground level for at least one computer cycle (1.75 μsec) after the start of the POT wait phase to ensure acknowledgment by the central processor. The wait phase terminates at the completion of that machine cycle during which the unit ready signal was acknowledged.

The following signals are generated by a POT instruction:

a. (Pot 1) - This signal is true during the entire wait phase of the POT instruction, and is false at all other times. (Pot 1) being true indicates to the external device that the C register output lines are stable and contain the 24-bit word to be transferred. (Pot 1) going false indicates to the external device that the computer has acknowledged the ready signal and has exited from the wait phase.

b. (Pot 2) - This signal is true from T5-T1 of every machine cycle during the POT wait phase, and is false at all other times. (Pot 2) may thus be used as a strobe by the external device to strobe the C register output lines ((C0) - (C23)). If a time-share operation occurs during the wait phase, the (Pot 1) signal will remain true, but (Pot 2) will be inhibited. At the completion of the time-share operation, depending upon the condition of ($\overline{Rt}$), at least one more cycle of wait phase will occur.

The following three signals are also generated by both the TMCC's and the DACC's, and are derived from the pulse counters in the communication channel. These timing signals may be used to clock Eom, Sys, Pot, etc., in an external device.

a. (Qq1) - This signal is true from T5 through T0 of every computer cycle, and is false at all other times.

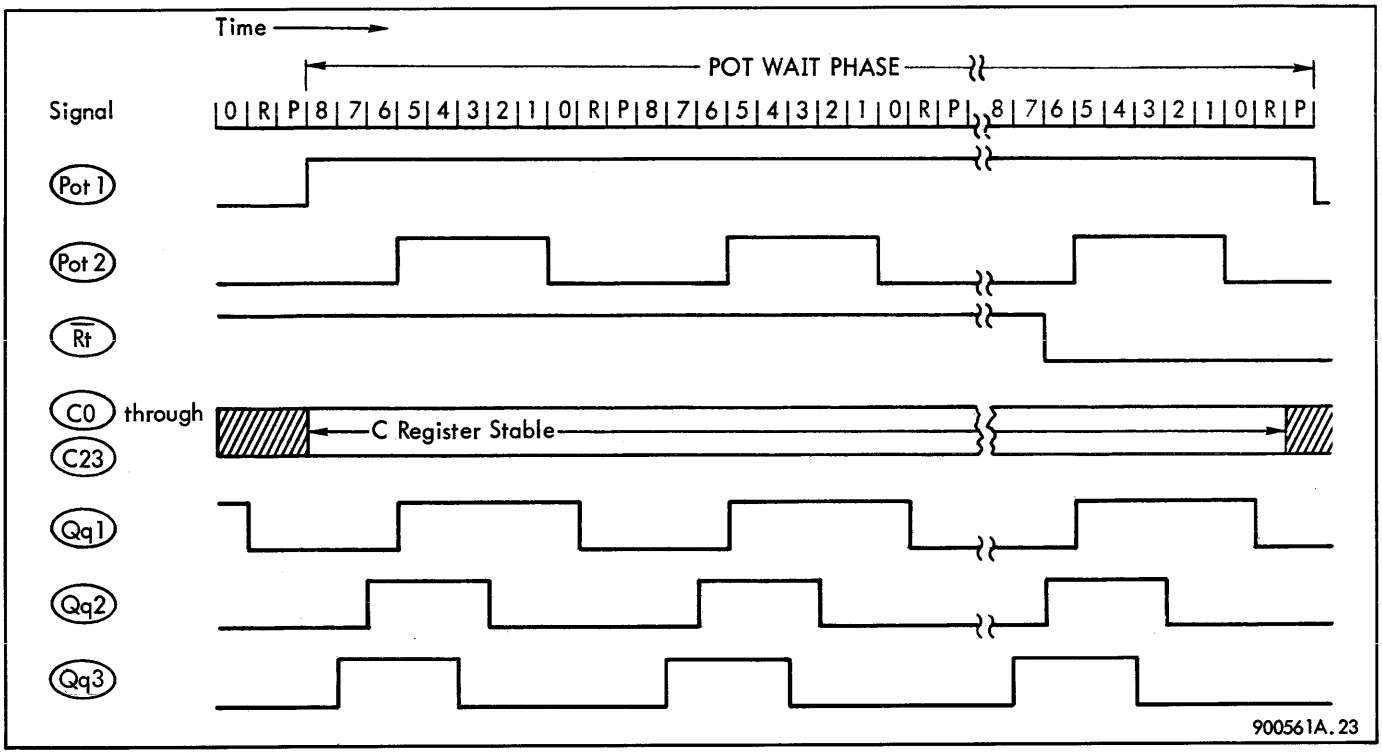


Figure 2-3. Signals Generated by POT Instruction

b. (Qq2) - This signal is true from T6 through T3 of every computer cycle, and is false at all other times. This signal may be used during the POT wait phase to indicate to the external device the time period during which the ready line (Rt) will be tested.

c. (Qq3) - This signal is true from T7 through T4 of every computer cycle, and is false at all other times.

PARALLEL INPUT (PIN)

The PIN instruction provides a means of direct parallel transfer of up to 24 bits of data from an external device into memory via the C register of the computer. Each word transferred is under direct program control. The PIN instruction must be preceded by an EOM instruction to select the desired device. During the execution of a PIN instruction the computer proceeds to a wait phase almost identical to that of a POT instruction. The wait phase consists of an integral number of computer cycles. The C register is first reset, then the input lines ((Cd0) - (Cd23)) are strobed into the C register. This process of resetting the C register and of then strobing the data repeats once every machine cycle during the wait phase of a PIN instruction.

When the ready signal is received ((Rt) going to ground level) from the external device, the computer exits from the wait phase and continues computation. The wait phase terminates at the completion of that machine cycle during which the external ready signal was acknowledged by the computer; therefore, a PIN instruction must go through at least one wait phase. The requirements for the ready signal are identical to those for a POT instruction. Thus, a PIN instruction requires 3 + n cycles [(5.25 μsec) + n (1.75 μsec)] where n = number of wait phases for execution.

NOTE

The C register input lines ((Cd0) - (Cd23)) are inverted before they are strobed into the C register; thus, the C register will receive the ones complement of the data impressed on (Cd0) - (Cd23).

PIN Interface Signals

Two signals are generated by a PIN instruction. See figure 2-4. These signals generated in the computer are available at the PIN connectors provided with each DACC and TMCC.

a. (Pin) - This signal is true from T7 through T0 of every computer cycle during a PIN wait phase and is false at all other times. (Pin) indicates to the external device that the C register input lines are being strobed into the C register and therefore must be stable at this time.

b. (Rti) - This signal is a 1.4 μsec ground level signal generated when the PIN instruction exits from the wait phase. (Rti) going to ground indicates to the external system that the CPU has acknowledged the ready signal by exiting from the wait phase and has accepted 24 bits of data. ((Rti) is positive in its quiescent condition).

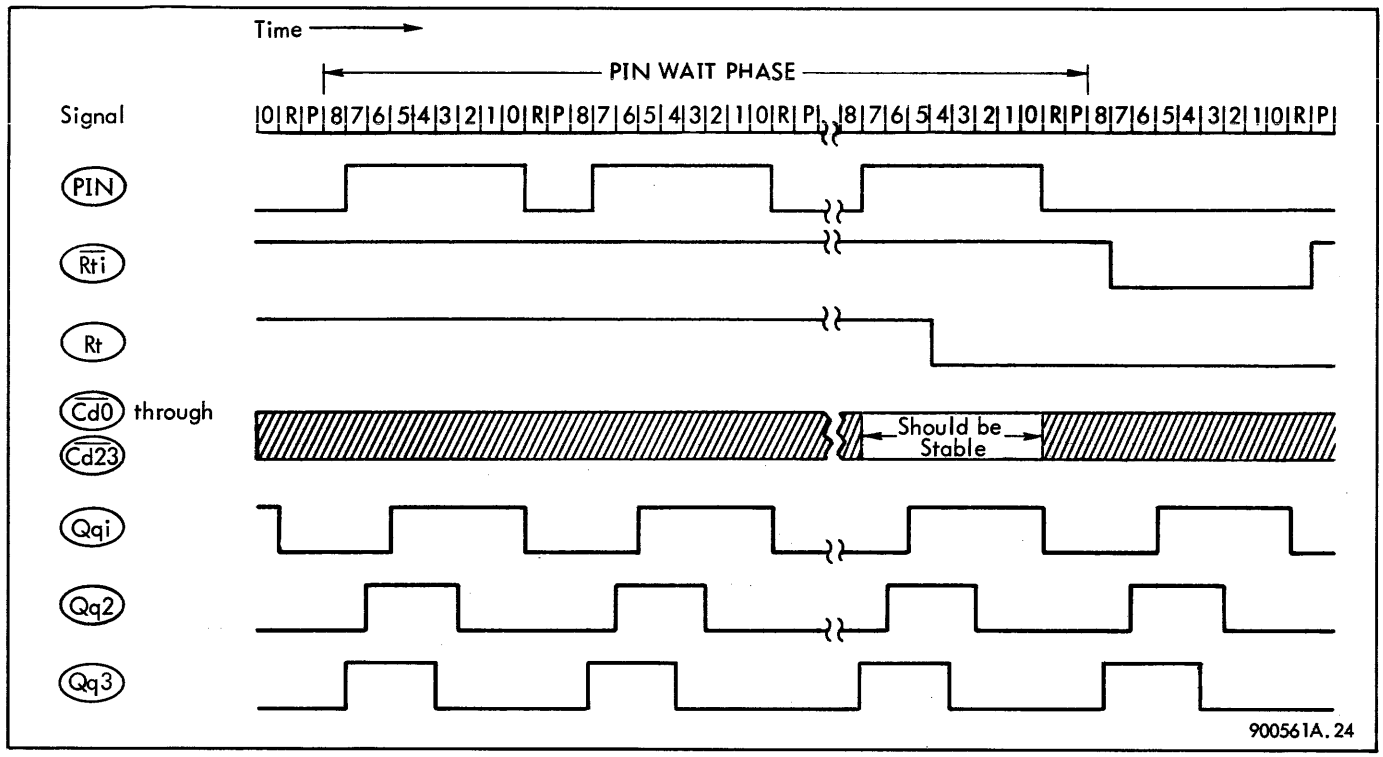


Figure 2-4. Signals Generated by PIN Instruction

If a time-share operation occurs during the wait phase, the Pin signal will be inhibited. At the completion of the time-share operation, depending on the condition of $\overline{Rt}$, at least one more cycle of wait phase will occur.

If a time-share operation occurs during the cycle after the last wait phase cycle, $\overline{Rti}$ will be inhibited until the completion of the time-share operation.

SDS 925 SPECIAL I/O OPERATIONS

The 925 Computer includes two additional I/O instructions, Block Parallel Output (BPO) and Block Parallel Input (BPI). These instructions are block transfer versions of POT and PIN instructions. The transmission of data is initiated by performing the following programming steps:

a. Load the number of words to be transferred, minus one, into the A register.

b. Alert the external unit by means of an EOM instruction.

c. Start the transfer with a BPO or BPI instruction.

The computer now enters a wait and transfer phase. If the external unit is ready, information will be transferred at a rate of one word each computer cycle (1.75 μsec) until the word count placed into the A register (which is counted down by one each I/O cycle) or until the external unit supplied the terminate signal $\overline{Bt}$.

Input (BPI)

The computer remains in the wait and data transfer phase until ready detector flip-flop, Rf, is set by the externally supplied ready signal $\overline{Rt}$. See figure 2-5.

$$sRf = (\emptyset 2\ \overline{O5}\ O6\ Tp)\ Rt$$
$$rRf = (\emptyset 2\ \overline{O5}\ O6\ Tp)\ \overline{Rt}$$

The computer supplies a Pin signal each time a word is being transferred into the C register.

$$Pin = (\emptyset 2\ O6)(T7\text{-}T0)\ \overline{Ts}\ O2\ Rf$$

This process continues until the word count reaches zero or until the external unit supplies a ground to the terminate signal line $\overline{Bt}$. Either condition causes the computer to exit from the wait and data transfer phase at pulse time Tp. The computer now generates the transfer complete signal $\overline{Rti}$.

$$Rti = (\emptyset 4\ \overline{O1}\ \overline{O4}\ O6)\ \overline{Ts}\ (T7\text{-}Tr)$$

If the external unit cannot supply information each 1.75 μsec, the ready signal line $\overline{Rt}$, can be used as a clock to synchronize the operations.

Output (BPO)

The computer enters the wait and data transfer phase and supplies the Pot1 signal. The external unit must supply the ready signal, $\overline{Rt}$, before the computer can generate the Pot2 signal. The $\overline{Rt}$ signal sets the ready detector

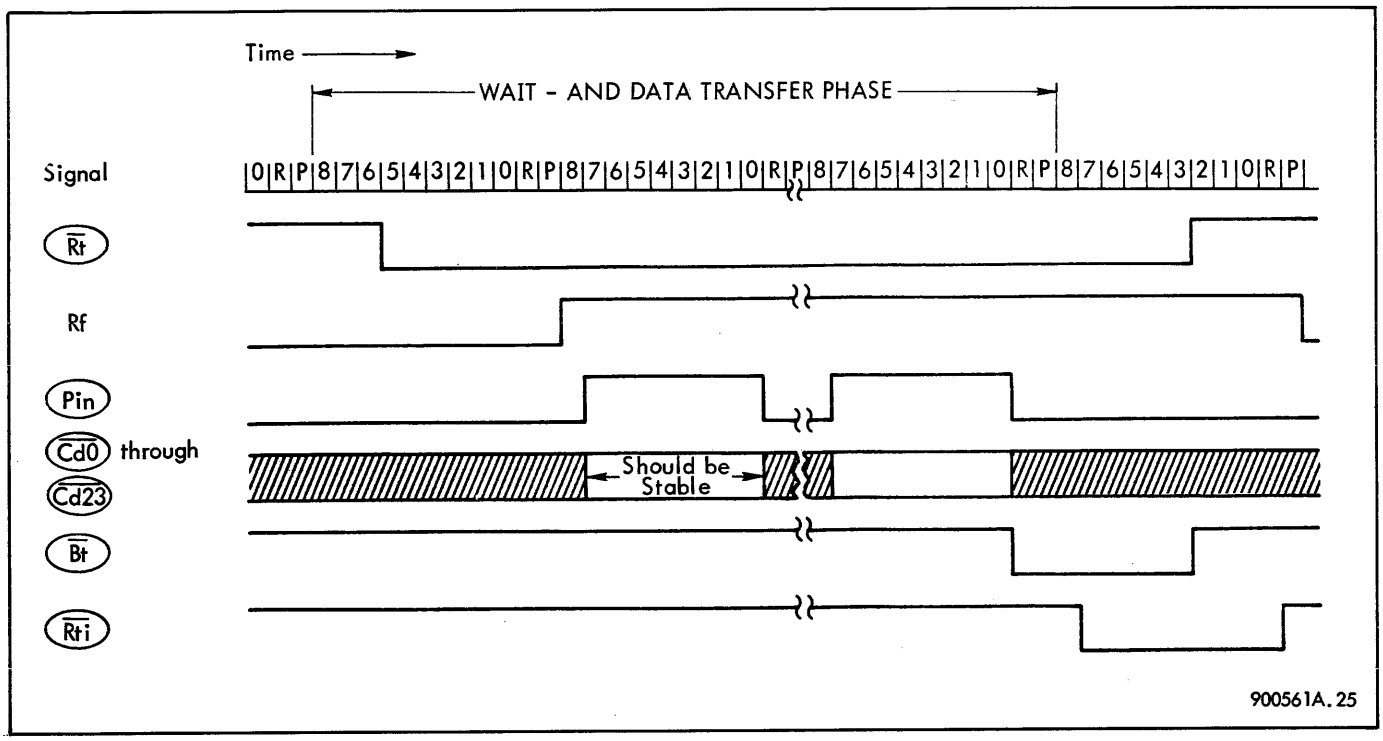


Figure 2-5. Signals Generated by 925 BPI Instruction

flip-flop Rf in the same manner as for block parallel inputs. See figure 2-6.

$$sRf = (Ø2\ \overline{O5}\ O6\ Tp)\ Rt$$

$$rRf = (Ø2\ \overline{O5}\ O6\ Tp)\ \overline{Rt}$$

$$(Pot2) = Pot1\ (T5\text{-}T1)\ Tsr\ Rf\ O5$$

The (Pot2) signal can be used by the external unit to strobe the C register outputs. This process continues until the word count reaches zero or the external unit supplies a ground on the terminate signal line ($\overline{Bt}$). ($\overline{Bt}$) is recognized at pulse time Tp, and therefore must be low for at least one cycle to ensure acknowledgement. Either condition causes the computer to exit from the wait and data transfer phase at pulse time Tp.

As in block input operations the ready signal line, ($\overline{Rt}$), can be used as a clock to synchronize the block parallel output operation.

SKIP IF SIGNAL NOT SET (SKS)

The SKS instruction provides a means of program sensing both internal and external conditions. This instruction operates in four basic modes that are program selectable by the setting of two bits (C10 and C11) within the SKS instruction format.

C10	C11	Mode
0	0	Special Internal Test
0	1	Channel/Device Test
1	0	Internal Test
1	1	System Test

Only channel/device test and system test are available to the external equipment, and will be described.

The SKS system test mode is divided into two submodes (system test external, and system test internal) by gating bit 9 with bits 10 and 11. This is necessary if the two submodes of the EOM system control are utilized. Refer to paragraph on system control EOM.

C1	C9	C10	C11	
X	0	1	1	SKS System Test (External)
X	1	1	1	SKS System Test (Internal)

The SKS instruction tests the status of signals supplied to the computer by peripheral devices or system equipment. If the signal is low, the next instruction in sequence is skipped. If this signal is positive, the program does not skip but continues in its normal sequence. C1 must always be included in the decoding circuitry since the term C1 separates the Data Multiplex System ($\overline{C1}$) from other I/O units (C1).

The SKS instruction requires two computer cycles (3.5 µsec) if no skip occurs, and three cycles (5.25 µsec) if a skip does occur.

SKS Interface Signals

The following signals necessary to implement the SKS tests are available at the I/O connectors on each TMCC and DACC. See figure 2-7.

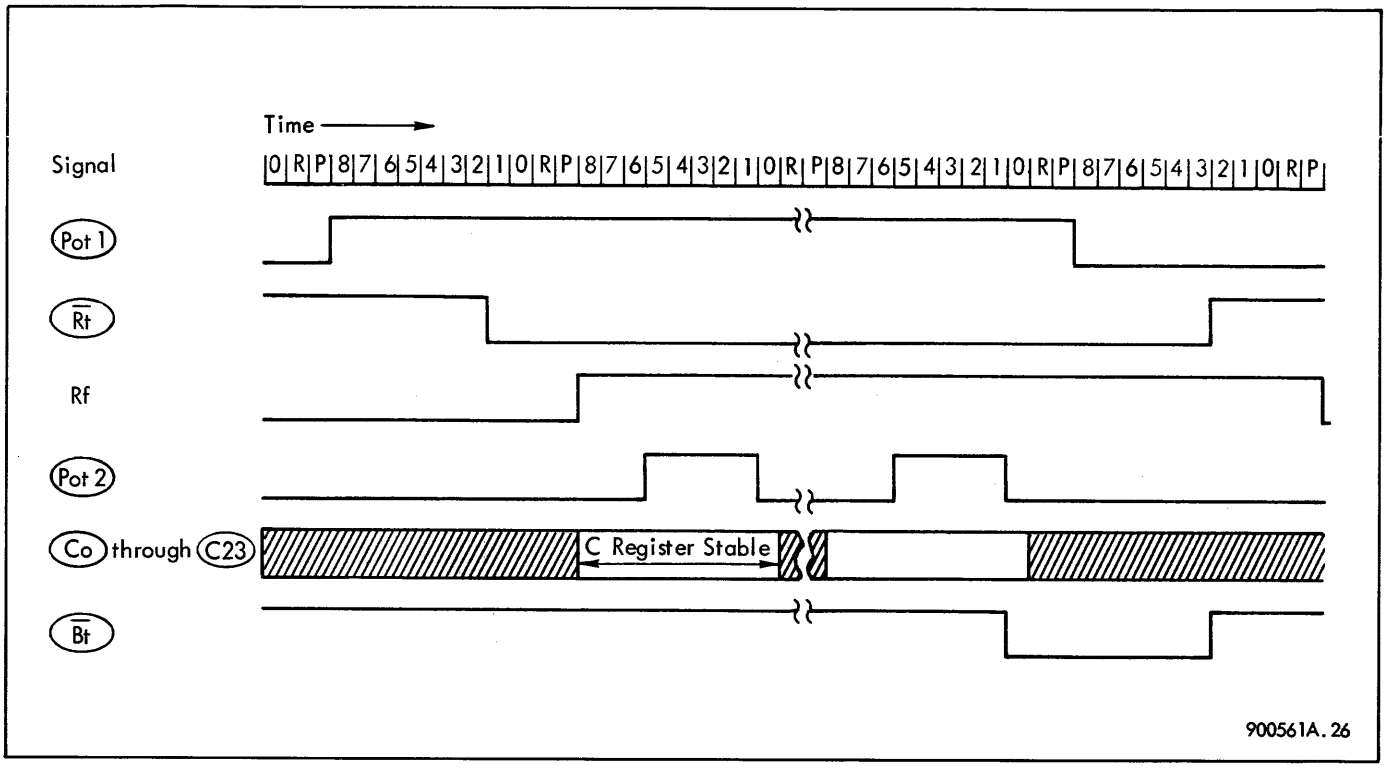


Figure 2-6. Signals Generated by 925 BPO Instruction

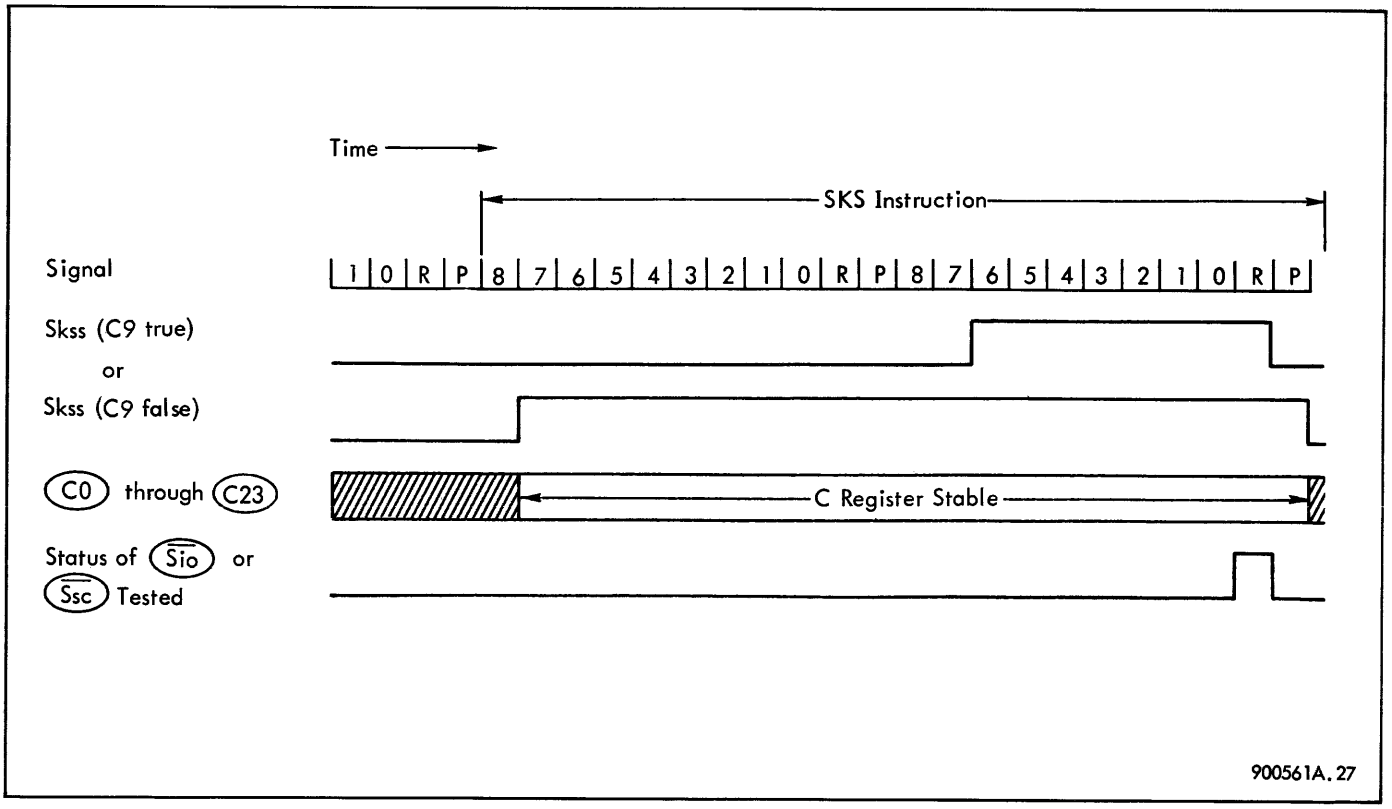


Figure 2-7. Signals Generated by SKS Instruction

a. (Skss) - This signal is generated by each SKS instruction and indicates that the C register outputs ((C1), (C9) through (C23)) are stable and may be decoded by external equipment prior to supplying the computer with the test signal. The external equipment should decode all available bits ((C1), (C9) through (C23)) since some configurations have been pre-assigned for use with standard equipment such as data multiplexing systems, message switching, etc.

The (Skss) signal is true from T6 - Tr of the second cycle of the SKS instruction if bit C9 is true. If bit C9 is false, (Skss) is true from T7 of the first cycle through Tr of the second cycle. (Skss) is inhibited during a time-share operation. If a time-share operation occurs during either of the first two cycles of an SKS instruction, both cycles will be repeated at the completion of the time-share operation.

b. ($\overline{\text{Sio}}$) - This signal is generated by peripheral devices when (Skss) is true during the SKS instruction, channel/device mode. The C register bits C1, C9, C10, and C11 are decoded internally and need not be decoded externally to determine channel/device mode. Bits C12 through C23 must be decoded to select the desired device. A zero volt condition on this line causes the computer to skip the next instruction in sequence.

c. ($\overline{\text{Ssc}}$) - This signal is generated by external system equipment when (Skss) is true during the SKS instruction, system mode. The C register bits C1 and C9 must be decoded externally to determine system test external mode with bits C12 through C23 providing the desired single-bit input address.

SECTION III INPUT/OUTPUT CHANNEL DESCRIPTION

GENERAL

This section describes the optional features, timing considerations, and interfacing requirements of the several input/output channels available to the SDS 925/930/9300 Computers - the TMCC, DACC, DMS, MIC, and Priority Interrupts.

TIME MULTIPLEXED COMMUNICATION CHANNEL (TMCC)

The TMCC is a time multiplexed input/output channel for communication between a peripheral device and the SDS 925/930/9300 Computers. Its operation is designated "time multiplexed" because it gains access to the computer memory through the same path utilized by the computer and must therefore momentarily interrupt computation to store or obtain a word of information. Up to four TMCC's may be connected to one computer and all may be active simultaneously. Since their operation is time multiplexed, however, only one channel at a time can communicate with the computer memory.

TMCC has two registers for data storage which provide the means to assemble input characters into words or to disassemble words into output characters. The TMCC communicates with the computer by means of a 24-bit Word Assembly Register (WAR) which transfers words between the TMCC and the computer's C register. The TMCC communicates with external systems by means of the bidirectional Single Character Register (SCR) using either a 6-, 12-, or 24-bit character format plus a parity bit. See figure 3-1. The character size depends on the optional registers that may be installed. The number of characters per word is under program control but is limited to a maximum of four 6-bit characters, two 12-bit characters, or one 24-bit character. Mode of transfer is serial by character, parallel by bit. A TMCC having the larger character-length options may be switched from one size to another under control of the external system. The length is selected by activating one of the control lines, (Wx12) or (Wx24). A particular device can activate only one of these lines; if none is activated, the TMCC assumes the 6-bit character format. The rate of information transfer is determined by the clock signal ($\overline{\text{Ecw}}$) from the external device. For both input and output, the TMCC will slave itself to the frequency of the device's clock.

Information may be input or output by executing an instruction for each word. The instruction may be given in advance of the time it is needed, in which case the computer remains idle until the channel is ready. Or the computer interrupt system may be used so that the channel can call for an instruction when it is ready. This allows the computer to continue with other computations when not actually engaged in the I/O process.

Unit Address Codes

Sixty-four unit address codes are available to the TMCC. Refer to table 3-1. Two of these codes (00 and 40) are reserved for channel disconnect. While the code 40 will disconnect the channel it is not generally used for this purpose since it does not reset W9 flip-flop as it disconnects.

The remaining 62 addresses are divided into 31 input device codes (W9), and 31 output device codes ($\overline{\text{W9}}$). When choosing a device code for equipment other than those listed in table 3-1, care must be taken that no code reserved for any magnetic tape operation or for paper tape input be used. If W11 is true (magnetic tape) the buffer will modify the normal terminate condition. If a paper tape input code is used, an all zero character (Rw1 - Rwp = 0) will cause a gap indication to the buffer.

Interlace

An optional interlace feature may be installed in the TMCC for either the W or Y channels to facilitate input/output operations with fewer instructions. The interlace logic allows a program to tell the TMCC how many words are to be transferred and the memory location of the first word. Then, with no further instructions, the TMCC will assemble or disassemble the number of words specified and call on the computer each time it is ready to transfer a word to or from memory. Thus, the I/O process may be interlaced with computation or with similar I/O operations on other channels.

Two additional registers are provided with the interlace feature:

a. Word Counter - a 15-bit counter used to store the number of words to be transferred during the interlace I/O operation. With each word transfer, one is subtracted from the number in the counter.

b. Address Counter - a 15-bit register used to store the address of the memory location currently being accessed. Each time a word is taken from or sent to memory, a one is added to the number in this register.

Input

A brief description of a non-interlaced process follows. The TMCC is initialized by an EOM instruction, buffer control

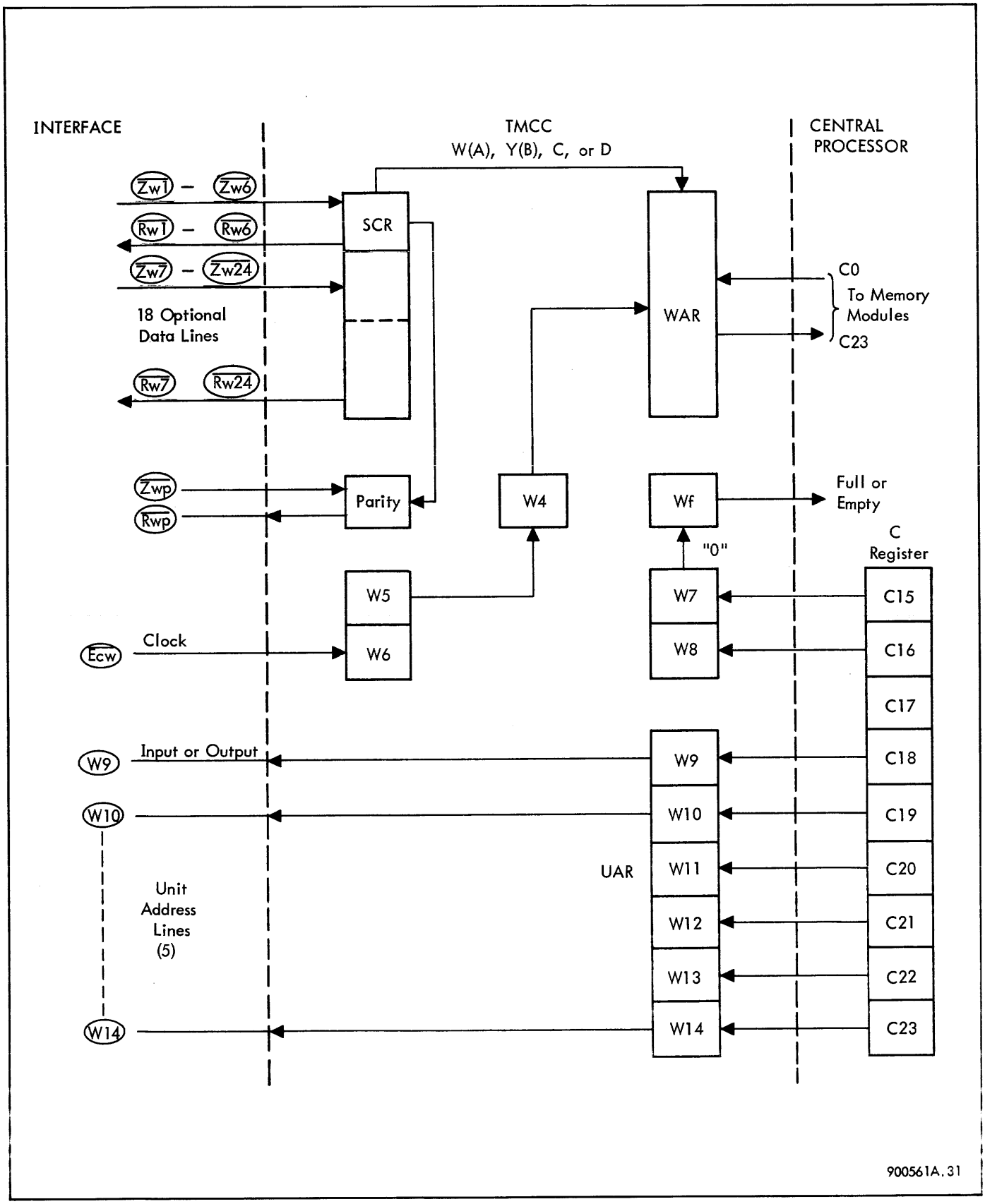


Figure 3-1. TMCC Simplified Block Diagram

Table 3-1. Unit Address Codes

Code	Unit	Code	Unit
00	Disconnect	40	
01	Type Input No. 1	41	Type Output No. 1
02	Type Input No. 2	42	Type Output No. 2
03	Type Input No. 3	43	Type Output No. 3
04	Paper Tape Input No. 1	44	Paper Tape Punch Output No. 1
05	Paper Tape Input No. 2	45	Paper Tape Punch Output No. 2
06	Card Reader Input No. 1	46	Card Punch Output No. 1
07	Card Reader Input No. 2	47	Card Punch Output No. 2
10	Magnetic Tape Input No. 0	50	Magnetic Tape Output No. 0
11	Magnetic Tape Input No. 1	51	Magnetic Tape Output No. 1
12	Magnetic Tape Input No. 2	52	Magnetic Tape Output No. 2
13	Magnetic Tape Input No. 3	53	Magnetic Tape Output No. 3
14	Magnetic Tape Input No. 4	54	Magnetic Tape Output No. 4
15	Magnetic Tape Input No. 5	55	Magnetic Tape Output No. 5
16	Magnetic Tape Input No. 6	56	Magnetic Tape Output No. 6
17	Magnetic Tape Input No. 7	57	Magnetic Tape Output No. 7
20	——	60	High-Speed Printer Output No. 1
21	——	61	High-Speed Printer Output No. 2
22	——	62	——
23	——	63	——
24	——	64	Incremental Plotter Output No. 1
25	——	65	Incremental Plotter Output No. 2
26	Disc File or Auxiliary Drum Input No. 1	66	Disc File or Auxiliary Drum Output No. 1
27	Disc File or Auxiliary Drum Input No. 2	67	Disc File or Auxiliary Drum Output No. 2
30	Scan Magnetic Tape No. 0	70	Magnetic Tape Erase No. 0
31	Scan Magnetic Tape No. 1	71	Magnetic Tape Erase No. 1
32	Scan Magnetic Tape No. 2	72	Magnetic Tape Erase No. 2
33	Scan Magnetic Tape No. 3	73	Magnetic Tape Erase No. 3
34	Scan Magnetic Tape No. 4	74	Magnetic Tape Erase No. 4
35	Scan Magnetic Tape No. 5	75	Magnetic Tape Erase No. 5
36	Scan Magnetic Tape No. 6	76	Magnetic Tape Erase No. 6
37	Scan Magnetic Tape No. 7	77	Magnetic Tape Erase No. 7

mode. This operation also places the address code for the external device into the Unit Address Register (UAR) and fills the character counter (W7, W8) with the number of characters per word count. Each external device decodes the UAR outputs (W9) through (W14) and prepares to send information to the TMCC when addressed. The unit address lines (W9) through (W14) are false when the TMCC is inactive. Once addressed, the external device generates a clock signal (Ecw) each time a character is ready to be transferred into the TMCC via the data input lines ($\overline{Zw1}$) through ($\overline{Zw24}$) and ($\overline{Zp}$). See figure 3-2. These data lines are inverted before they are strobed into the character register, thus the ones complement of the data placed on ($\overline{Zw1}$) through ($\overline{Zw24}$) will be received.

$$sRw1 = \overline{W9}\ W6\ \overline{W5}\ Zw1 + - - -$$

$$sRw24 = \overline{W9}\ W6\ \overline{W5}\ Zw24 + - - -$$

The input data is strobed into the single character register until flip-flop W5 is set. It will be shown later that W5 will set after the input clock signal ($\overline{Ecw}$) has been removed.

The TMCC monitors the ($\overline{Zwp}$) input line, checking for parity errors after information is strobed into the single character register. If an error is detected, the error indicator flip-flop, We, is set. The status of this flip-flop can be tested by the program. If the external device does not generate the parity bit (odd parity is used), the parity checking feature can be inhibited by making the interface line (Npw) low during data transfer.

The quiescent state of the signal clock ($\overline{Ecw}$) is positive. To initiate a data transfer, ($\overline{Ecw}$) must first go low to set clock detector flip-flop W6.

$$sW6 = \overline{W5}\ Ecw\ T8$$

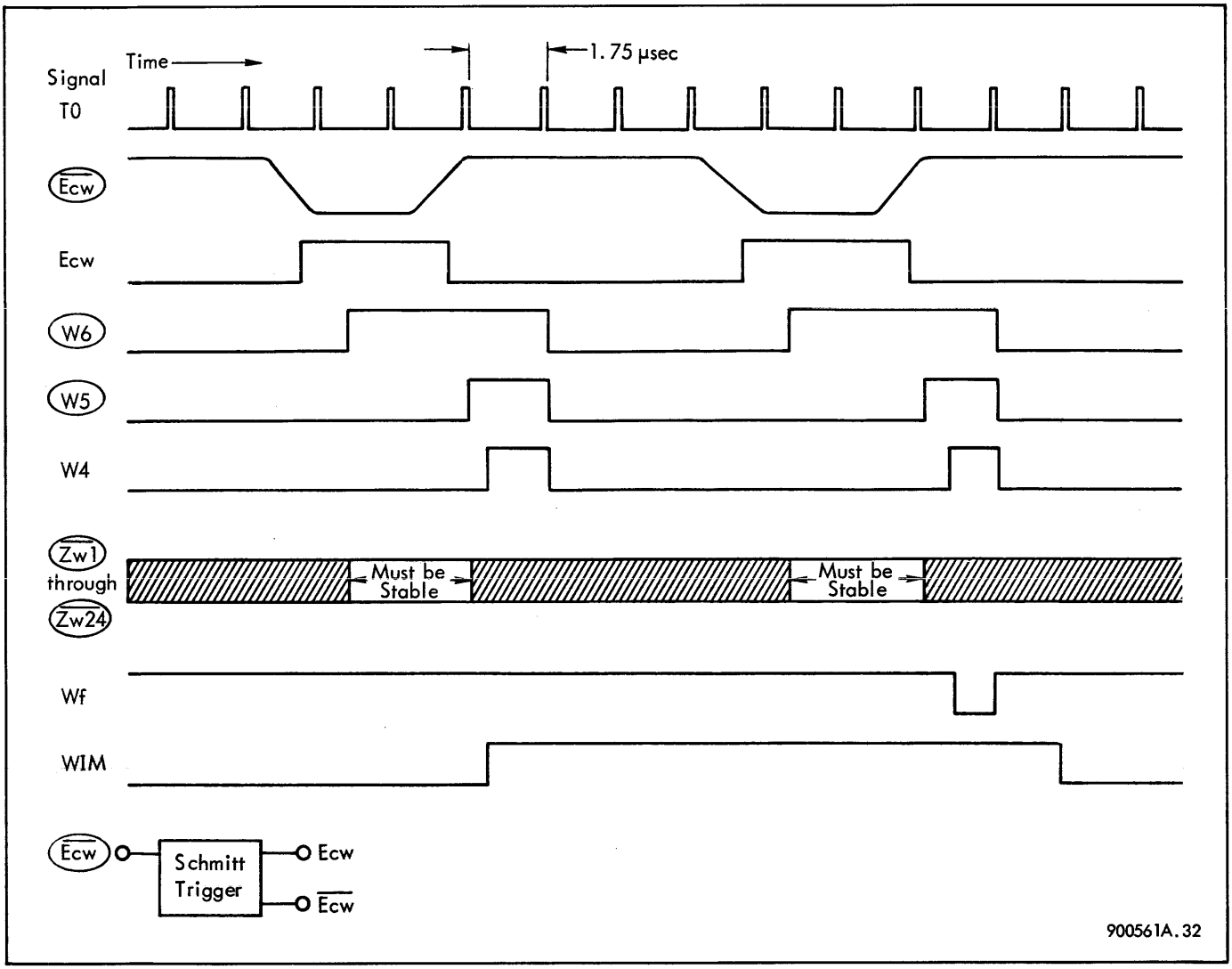


Figure 3-2. Input Timing Characteristics Asynchronous Mode

After W6 is set, the character register is filled

$$sRw1 = Zw1\ \overline{W9}\ \overline{W5}\ W6\ +\ -\ -\ -$$
$$\vdots \qquad\qquad \vdots$$
$$sRw24 = Zw24\ \overline{W9}\ \overline{W5}\ W6\ +\ -\ -\ -$$

and the precess detector flip-flop W5 is set after $\overline{Ecw}$ goes high.

$$sW5 = \overline{W5}\ W6\ \overline{Ecw}\ T0$$

The contents of the SCR are now ready to be shifted into the word assembly register under control of flip-flop W4 providing Wf is true.

$$sW4 = W5\ Wf\ T8\ \overline{Wg}$$

The Wf signal will be false if the WAR is not able to accept data (the computer has not yet serviced the previous word in WAR because of a higher priority channel requiring access, or because the WIM command has not yet been given).

After the shift, W4, W5, W6 and the SCR are reset in preparation for reception of the next character from the external device.

$$rW4 = W4\ T0$$
$$rW5 = W4\ T0$$
$$rW6 = W5\ T0$$
$$rRw1 = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$$
$$\vdots \qquad\qquad \vdots$$
$$rRw6 = \overline{W9}\ \overline{W6}\ \overline{W5}\ \overline{W4}$$

This process repeats until the proper number of characters (indicated by the character count register) have been shifted to the Word Assembly Register (WAR). The "buffer full" flip-flop, Wf, is then reset to indicate to the computer that a word has been assembled and is ready for transfer to memory.

The WIM instruction will perform the actual transfer when the interlace feature is not available. If the WIM instruction occurs before Wf is reset, the computer program will be delayed until the TMCC is full and Wf is reset. If the WIM instruction occurs too late (i.e., after the SCR is ready to shift another character into the WAR) the error detector flip-flop, We, is set.

Input Clock Characteristics

The Ecw signal from the device indicates to the channel that the character in the SCR has been accepted by the device. Each time a character is accepted by the device (Ecw), the next character is shifted into the SCR unless the character accepted by Ecw was the last character to be output from the channel. If the accepted character was the last character, W6 and W5 will set, W6 will reset, but W5 will remain set resulting in the halt interlock condition $\overline{W0}\,W5\,\overline{W6}$.

If the channel is activated to output with no leader (the usual case for output), W5 is set by the Buc-type EOM instruction. W5 will remain set until the word has been transferred from the computer to the channel buffer and the first character is in the character register. When the transfer is complete W5 will reset. When W5 is false the device recognizes that the first output character is ready.

If the channel is activated to output with leader, W5 is reset, indicating to the output device that the character is ready. The character register and the parity output are in the reset condition.

Figure 3-2 shows the characteristics of a typical input clock signal and its relationship to the input data and clock counter flip-flops. An examination of this figure and the equations for W4, W5 and W6 will show that if the data is sampled by W6 $\overline{W5}$ it should be stable during this time.

Figure 3-3 illustrates two detailed examples of the clock signal, $\overline{Ecw}$. In examining these figures, bear in mind that to be assured of a timing pulse occurring during the off (to set W6) and on (to set W5) periods of $\overline{Ecw}$, each of these periods must be at least one machine cycle in length. This prescribes an input clock cycle of no less than two machine cycles. Actually, the clock rate must be somewhat slower than this for proper operation of W6, W5, and W4. Figure 3-3a shows two input clocks with timing such that the second clock is missed. Ideally, any clock rate slower than that of figure 3-3a would be satisfactory; however, a safety margin must be provided to compensate for noise and variations in waveshape and frequency. The input frequency may be increased as shown in figure 3-3b if the clocks are interlocked with W5 and W6 such that

$$\overline{Ecw} = \overline{\overline{W5}\ \overline{W6}\ \text{Device Clock}}$$

In this case, only two machine cycles per input clock are needed. Some of the peripheral device couplers already include this feature. Gating the device clock with W5 W6 does not necessarily mean that the $\overline{Ecw}$ signal will appear to by synchronous in respect to itself; that is, that it will always be low for the same time duration. $\overline{Ecw}$ can be low for as much as seven pulse times or for as little as a single pulse time, depending upon when the device clock falls in relationship to pulse time T8.

If the clock rate is too fast, the error detector flip-flop will be set.

$$sWe = W0\ \overline{W6}\ W5\ Ecw\ T8 + - - -$$

This equation, in effect, says that an error indication will occur if the clock signal $\overline{Ecw}$ is received before the previous character has been shifted out of the character register. When the interlock feature of figure 3-3b is employed, the condition W6 W5 Ecw cannot occur to set We. Under such circumstances, the external device must be capable of detecting its own rate errors and reporting them via the $\overline{Wes}$ line available to the interface connector.

$$sWe = Wes + - - -$$

The $\overline{Wes}$ line can be used for indicating an error condition by an external device during either input or output operations. Input timing characteristics with synchronous clock is shown in figure 3-4.

Input Termination

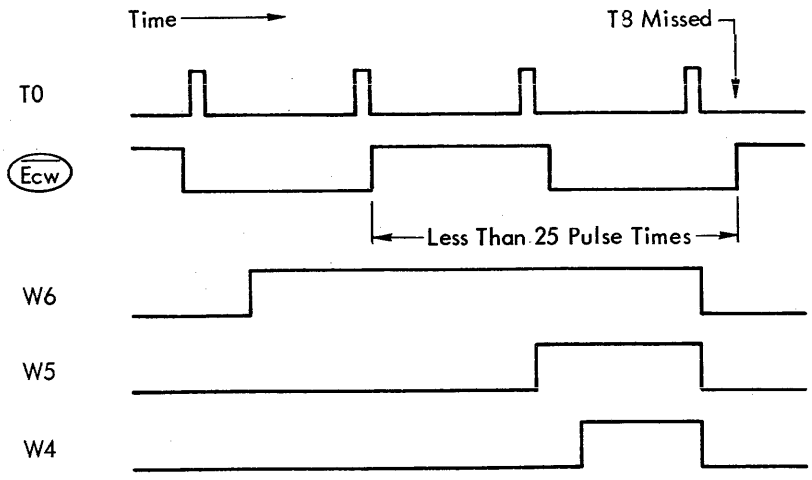
Terminating an input operation can take place in one of several ways. The simplest procedure is to program an EOM instruction to disconnect the external device after a predetermined number of WIM instructions have been processed. Special logic within the TMCC will cause automatic disconnect of paper tape input when "Leader" (all zeros) is read.

A more common method of terminating inputs is by external control of the end-of-record line, $\overline{Whs}$. The $\overline{Whs}$ line when held low (0 volts) by the external device will cause the TMCC disconnect sequence.

Output Timing

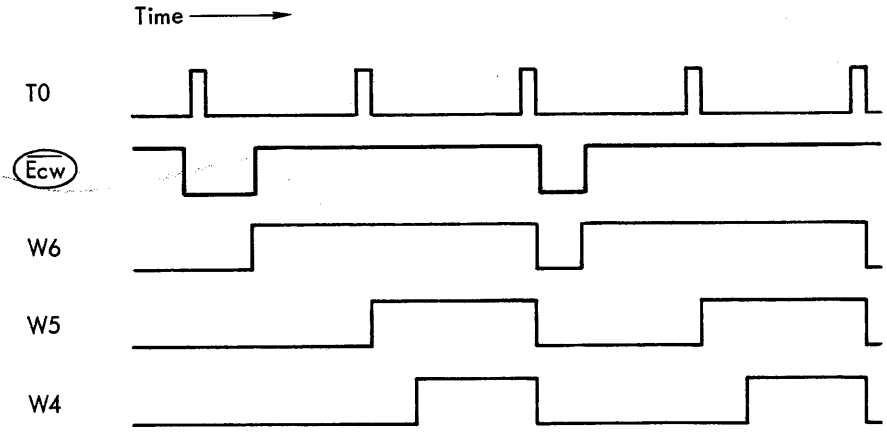
An EOM instruction, buffer control mode, enables the TMCC for outputs in a manner similar to that described for inputs. The EOM instruction must be followed closely by a MIW instruction to fill the Word Assembly Register (WAR). The external device must again decode the unit address register outputs, W9 through W14, before supplying output clock signals. The clock signal, $\overline{Ecw}$ characteristics are the same as for inputs and should be interlocked with TMCC terms, $\overline{W5}$ and $\overline{W6}$, to prevent clock signals at excessive rates and to prevent clocks before the word assembly register is filled. See figure 3-5.

The single character register outputs, Rw1 through Rw24, and parity output Rwp, are initially set false. For outputs requiring "leader" (such as for paper tape punch) these outputs will remain false until the external device supplies a clock signal.



a

Input clocks too fast. Asynchronous Mode



b

Input clocks interlocked with $\overline{W5}$ $\overline{W6}$ Synchronous Mode

900561A.33

Figure 3-3. Input Clock Timing Diagram

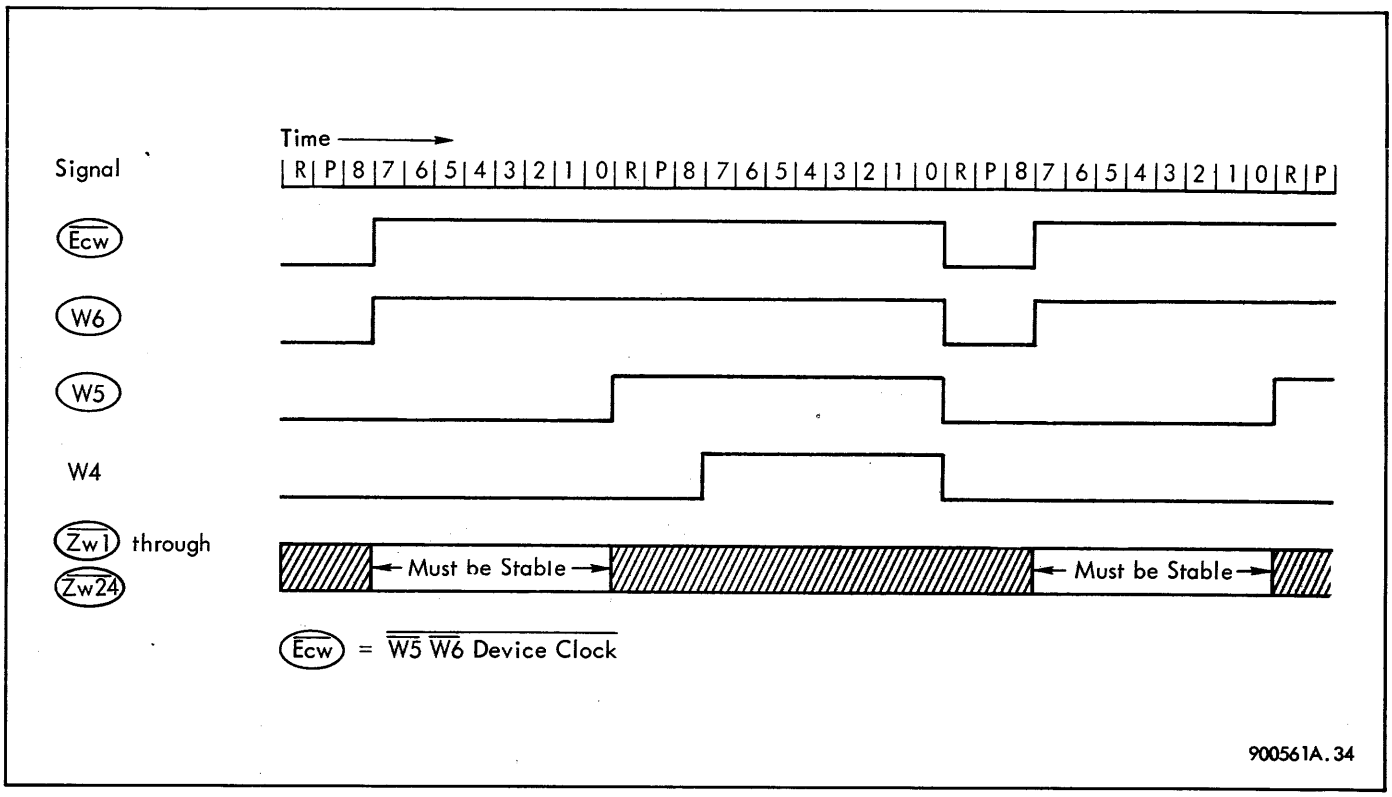


Figure 3-4. TMCC Input Timing, Synchronous Clock

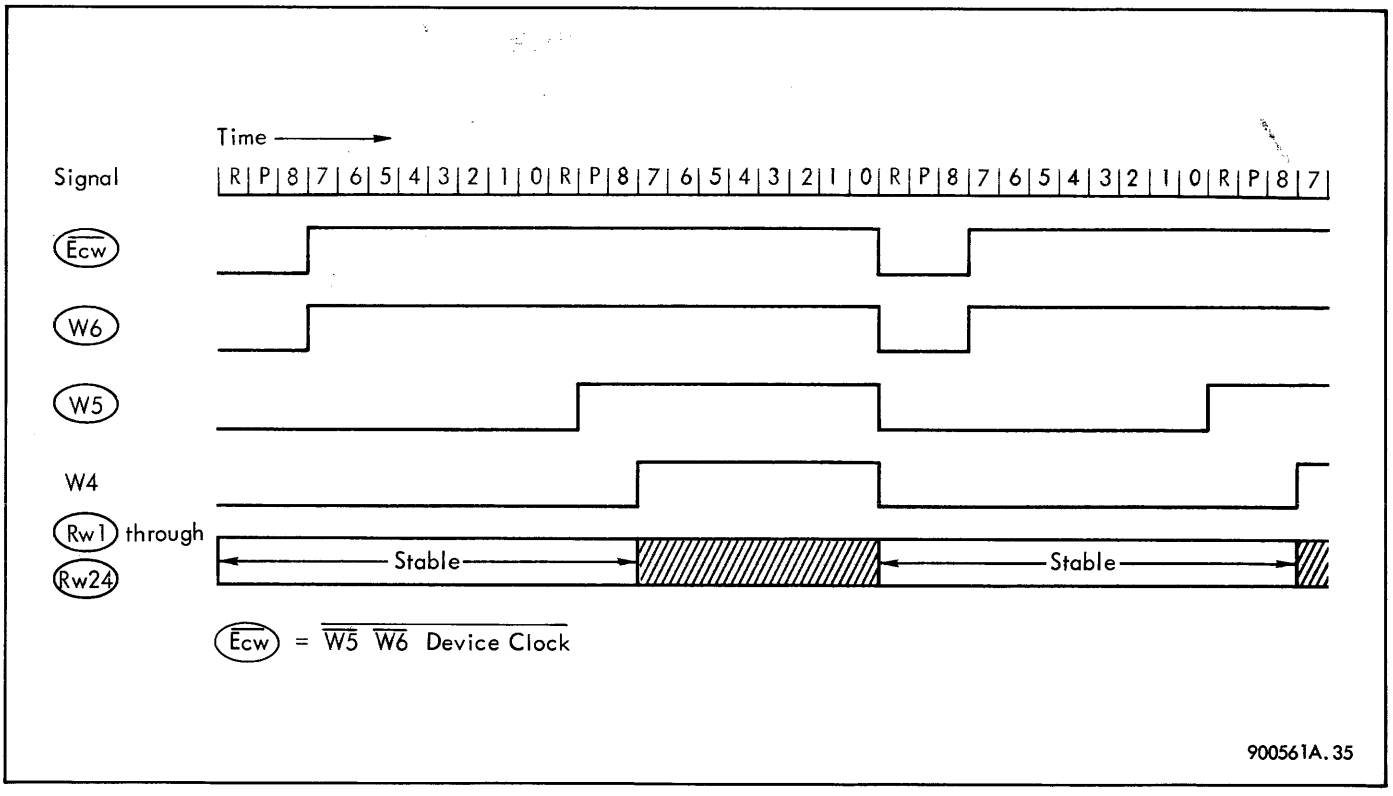


Figure 3-5. TMCC Output Timing, Synchronous Clock

Where "leader" is not requested, the first character is processed into the SCR immediately after the MIW instruction. In this case W5 will be true until the SCR is filled.

An odd parity bit is generated by the TMCC for each output character.

Output Termination

Terminating an output can be accomplished in several ways. The simplest method is to follow the MIW instruction which loads the last output word into the WAR with a "terminate output" EOM instruction. The TMCC will automatically disconnect after the last character has been accepted by the external device. The end-of-record line $\overline{Whs}$ will also cause automatic disconnect if held low by the external device.

Three signals generated by the TMCC can be combined by the external device to recognize when the last character has been transmitted.

$$\text{Halt Interlock Signal} = W5\ \overline{W6}\ \overline{W0}$$

The halt interlock signal can be used to alert the external unit to send the end-of-record response signals such as $\overline{Whs}$ and $\overline{Wes}$ to the TMCC.

Interlace Operation

The interlace feature provides the TMCC with a means for transferring blocks of words without requiring a separate instruction for each word to be transferred. The interlace operation falls into two categories - compatible and extended. The two modes differ basically in the methods used for terminating an input/output process. The compatible mode is directly compatible with the SDS 920 Computer. The types of interrupts that can be requested in the compatible mode are the End-of-Word and End-of-Transmission interrupts. The extended mode expands the I/O capability to include additional termination methods utilizing count-equal-zero and end-of-record interrupts. The I/O mode is selected by the binary state of bit 12 of the EOM instruction, where bit 12 = 0 causes the system to operate in the compatible mode, and where bit 12 = 1 causes the system to operate in the extended mode.

As far as the interface signals are concerned, the compatible mode allows the TMCC to operate in the manner described previously. However, the extended mode provides additional terminating options as outlined in table 3-2. The method of terminating is determined after the interlace has been alerted by bits 15 and 16 of the EOM instruction.

Table 3-2. Interlace Extended Mode Terminal Functions

Terminal Function	EOM Instruction C12	C15	C16	Summary of Operation
IORD Input/output of record then disconnect.	1	0	0	The I/O operation proceeds until the word count equals zero then terminates. On input, the channel disconnects when the End-of-Record is encountered. On output, the channel signals the device that the last character has been transmitted then disconnects after the device provides an End-of-Record response.
IOSD Input/output until signal then disconnect.	1	0	1	The channel disconnects when the word count equals zero or at the end of a record.
IORP Input/output of a record then proceed.	1	1	0	The I/O operation proceeds until the word count equals zero but does not terminate. On input, the channel sets the inter-record indicator when the end of a record is encountered. On output, the channel signals the device that the last character has been transmitted then sets the inter-record indicator after the device provides an End-of-Record response. The channel does not disconnect (except for magnetic tape when not programmed to continue).
IOSP Input/output until signal then proceed.	1	1	1	When the word count equals zero, the program should either reload the interlace to continue, or terminate the operation before the next clock is received; otherwise a rate error will occur.

DIRECT ACCESS COMMUNICATION CHANNEL (DACC)

The DACC provides a means of direct memory access by a communication channel, under interlace control, either simultaneous or time multiplexed with computation. The memory access will be simultaneous with computation if the memory bank to be accessed by the channel is not being accessed in computation. If the memory bank to be accessed by the channel is being accessed by the control processor, the transfer will be time multiplexed with computation. The SDS 925 is limited to one memory bank, and therefore all input/output operations in this computer are time multiplexed with computation.

The operation and interface signals for the DACC are similar to the TMCC with interlace. In fact, external units designed to operate with the TMCC are completely compatible and will operate with the DACC (normal mode). Refer to figures 3-6 and 3-7 for timing consideration of the DACC normal mode operation both asychronous and synchronous.

The DACC, however, does have some additional features described in the following paragraphs.

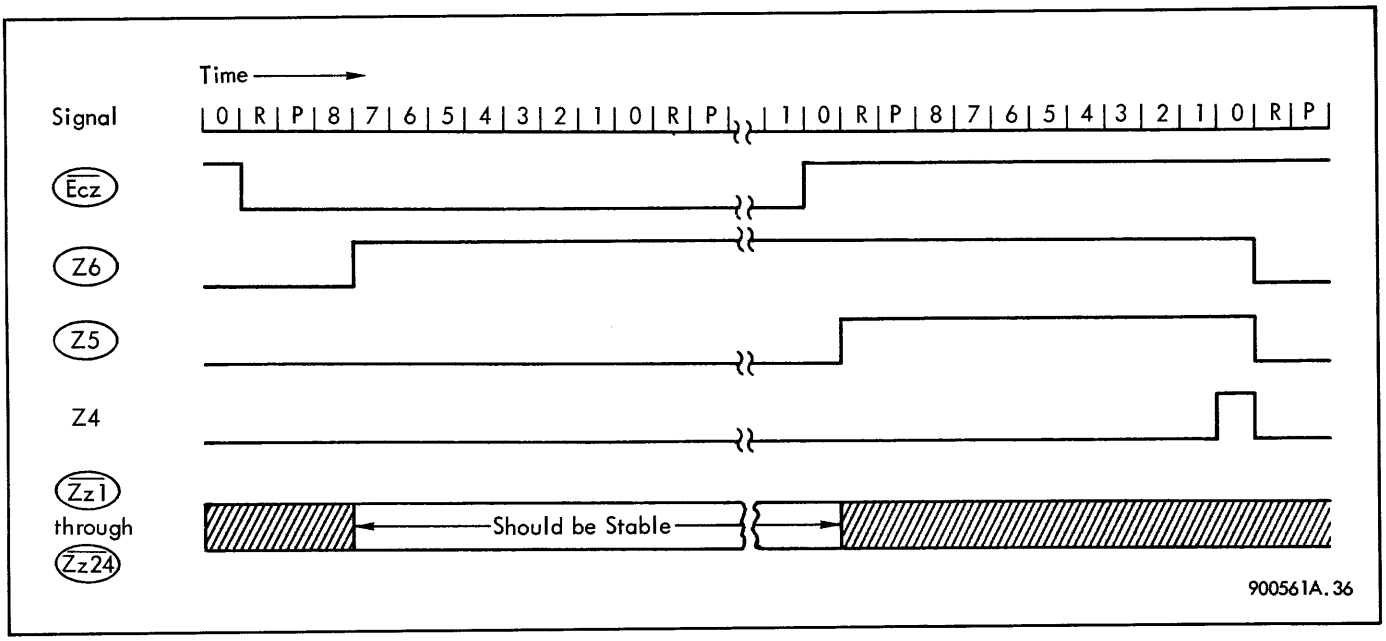


Figure 3-6. DACC Timing, Asynchronous Input Mode

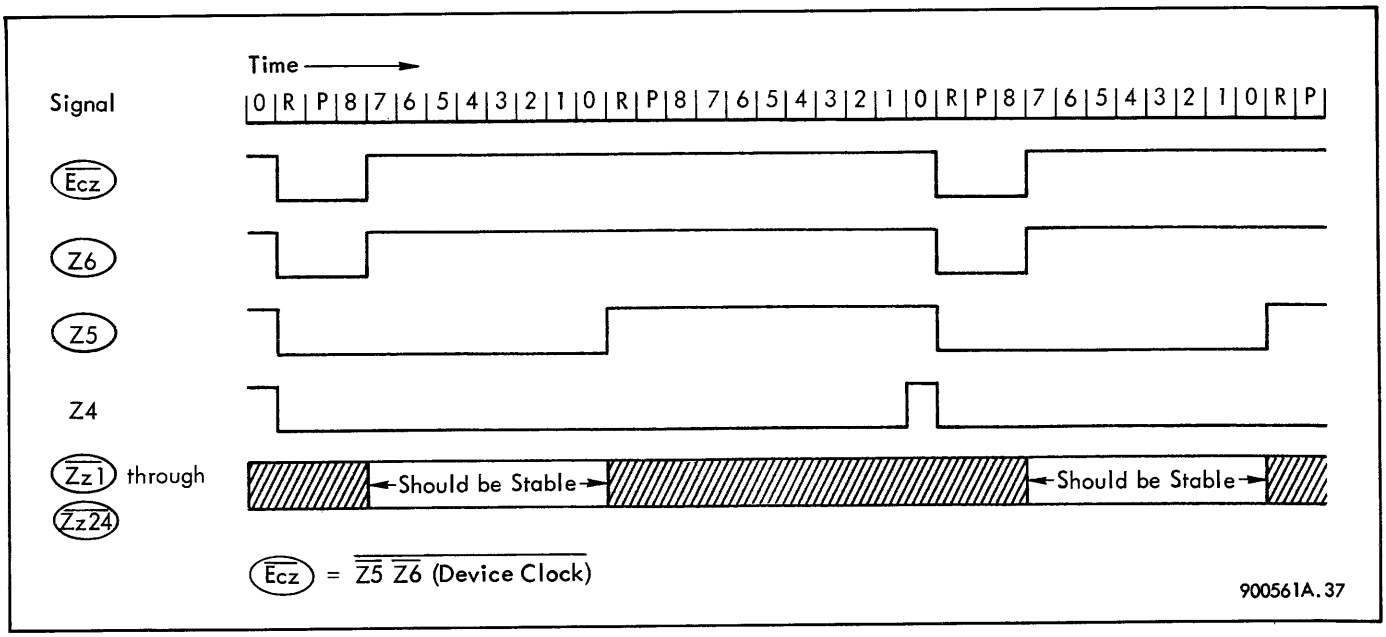


Figure 3-7. DACC Timing, Synchronous Input Mode

The DACC communicates with an external system by means of a bidirectional 24-bit shift register using 6-, 8-, 12-, or 24-bit characters plus a parity bit. The character size is selected by the external device through activation of one of the control lines, $\overline{Zx8}$, $\overline{Zx12}$, or $\overline{Zx24}$. A particular device is allowed to activate only one of the lines at any time and does so by causing the line to become false (low) while the device is addressed. If none of the lines is activated when an I/O unit is addressed, the DACC assumes a 6-bit character format. The characters thus transferred are assembled on input, or disassembled on output, in accordance with a word length which is under program control. The computer word contains 24 bits and the programmer may assign any number of characters per word which is within this limit (e.g. a maximum of three 8-bit characters per word). When an input word contains less than the maximum number of characters, the unused bits (in the most significant positions) are undefined. The rate of information transfer is controlled by the input clock signal, $\overline{Ecz}$, supplied by the external device. For both input and output, the DACC will slave itself to the frequency of $\overline{Ecz}$.

Information transfers can occur in either a normal mode or a high-speed mode. The rate is selected by the external device through activation of the high-speed select line, $\overline{Zft}$. When operating in the normal mode, the clock signal $\overline{Ecz}$, is treated by the DACC in the same manner as it is in the TMCC. However, if the high-speed select line $\overline{Zft}$ is held false by the external equipment, the clock detector flip-flops, Z5 and Z6, are able to set and reset immediately as the clock goes true and false without waiting for specific pulse times.

$$sZ6 = \overline{Z5}\ Ecz\ (- - - + Zft)$$

$$rZ6 = Z5\ (- - - + Zft)$$

$$sZ5 = \overline{Z5}\ Z6\ \overline{Ecz}\ (- - - + Zft)$$

$$rZ5 = Z4\ (\overline{Zx12} + Z15)$$

Under these conditions, the input/output rate can be increased from one character every 2 computer cycles to one character every 4 clock periods. Refer to figure 3-8. The input rate of fully assembled words into memory from the DACC cannot exceed the memory cycle time (1.75 μsec). Therefore, in the high-speed mode, care must be taken that the transfer rate of fully assembled words is not greater than one every 1.75 μsec. The DACC memory transfer must be synchronous with the computer cycle, and although five characters can be clocked every two cycles, the maximum transfer rate for 4-character words cannot exceed one transfer every two cycles.

The interface signal lines must be treated differently when operating in the high-speed mode. Typical signal transmission considerations are discussed in Section IV.

The DACC may terminate input/output operations in one of four modes. The mode of operation is established by the EOD instruction that enables the DACC (Bits 15 and 16). Table 3-3 describes these four terminating modes. The external device must respond to the $\overline{Z0}$ Z5 $\overline{Z6}$ condition in certain modes by providing an end-of-record signal, $\overline{Zhs}$.

Input/output connectors for the TMCC and the DACC (normal speed) assume external units with preassigned unit address codes. Table 3-4 list these standard codes. The unit address register can address a maximum of 31 input devices and 31 output devices; the unit address code 00 is reserved for channel disconnect purposes. Interface

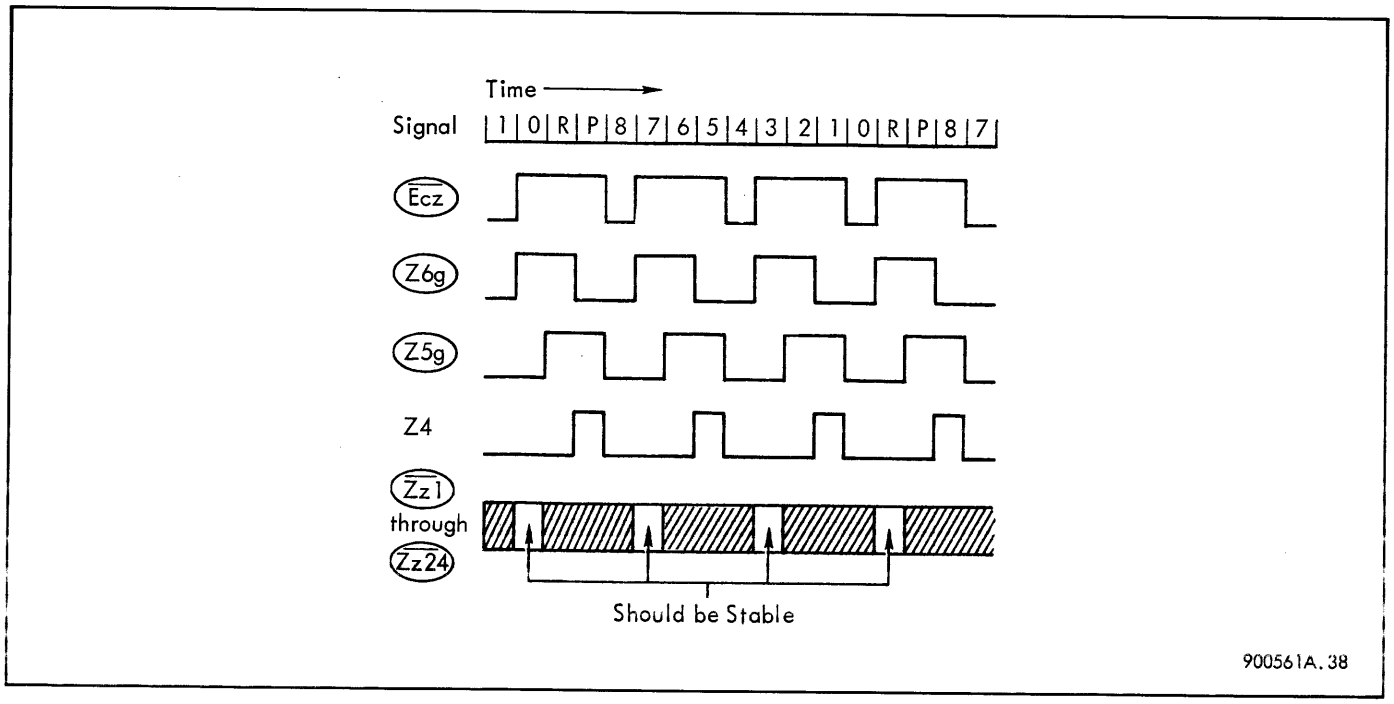


Figure 3-8. DACC Timing, High-Speed Synchronous Input Mode

Table 3-3. DACC Terminal Functions Extended Mode

Terminal Function	EOD Instruction C15	EOD Instruction C16	Summary of Operation
IORD Input/output of record then disconnect	0	0	The I/O operation proceeds until the word count equals zero then terminates. On input, the channel disconnects when the End-of-Record is encountered. On output, the channel signals the device that the last character has been transmitted then disconnects after the device provides an End-of-Record response.
IOSD Input/output until signal then disconnect	0	1	The channel disconnects when the word count equals zero or at the end of a record.
IORP Input/output of a record then proceed.	1	0	The I/O operation proceeds until the word count equals zero but does not terminate. On input, the channel sets the inter-record indicator when the end of a record is encountered. On output, the channel signals the device that the last character has been transmitted then sets the inter-record indicator after the device provides an End-of-Record response. The channel does not disconnect (except for magnetic tape when not programmed to continue).
IOSP Input/output until signal then proceed.	1	1	When the word count equals zero, the program should either reload the interlace to continue, or terminate the operation before the next clock is received; otherwise a rate error will occur.

Table 3-4. Unit Address Codes

Code	Unit	Code	Unit
00	Disconnect	40	
01	Type Input No. 1	41	Type Output No. 1
02	Type Input No. 2	42	Type Output No. 2
03	Type Input No. 3	43	Type Output No. 3
04	Paper Tape Input No. 1	44	Paper Tape Punch Output No. 1
05	Paper Tape Input No. 2	45	Paper Tape Punch Output No. 2
06	Card Reader Input No. 1	46	Card Punch Output No. 1
07	Card Reader Input No. 2	47	Card Punch Output No. 2
10	Magnetic Tape Input No. 0	50	Magnetic Tape Output No. 0
11	Magnetic Tape Input No. 1	51	Magnetic Tape Output No. 1
12	Magnetic Tape Input No. 2	52	Magnetic Tape Output No. 2
13	Magnetic Tape Input No. 3	53	Magnetic Tape Output No. 3
14	Magnetic Tape Input No. 4	54	Magnetic Tape Output No. 4
15	Magnetic Tape Input No. 5	55	Magnetic Tape Output No. 5
16	Magnetic Tape Input No. 6	56	Magnetic Tape Output No. 6
17	Magnetic Tape Input No. 7	57	Magnetic Tape Output No. 7
20	——	60	High-Speed Printer Output No. 1
21	——	61	High-Speed Printer Output No. 2
22	——	62	——
23	Full Word Input	63	Full Word Output
24	——	64	Incremental Plotter Output No. 1
25	——	65	Incremental Plotter Output No. 2
26	Disc File or Auxiliary Drum Input No. 1	66	Disc File or Auxiliary Drum Output No. 1
27	Disc File or Auxiliary Drum Input No. 2	67	Disc File or Auxiliary Drum Output No. 2
30	Scan Magnetic Tape No. 0	70	Magnetic Tape Erase No. 0
31	Scan Magnetic Tape No. 1	71	Magnetic Tape Erase No. 1
32	Scan Magnetic Tape No. 2	72	Magnetic Tape Erase No. 2
33	Scan Magnetic Tape No. 3	73	Magnetic Tape Erase No. 3
34	Scan Magnetic Tape No. 4	74	Magnetic Tape Erase No. 4
35	Scan Magnetic Tape No. 5	75	Magnetic Tape Erase No. 5
36	Scan Magnetic Tape No. 6	76	Magnetic Tape Erase No. 6
37	Scan Magnetic Tape No. 7	77	Magnetic Tape Erase No. 7

signals (W9) or (Z9), when true, designate output function. Although external equipment of many other types can be connected to these connectors, certain address restrictions exist. The restrictions result because partial control for the paper tape reader and the magnetic tape is contained within the channel logic. Care must be used if the addresses preassigned to these devices are used for other purposes.

MEMORY INTERFACE CONNECTION (MIC)

The MIC provides a direct access channel to the computer memory under external control. The MIC communicates with external equipment and with the computer by words of 24 parallel bits plus a parity bit. With the external equipment providing the memory address and input/output indicator, the following operations occur each time a direct access is requested.

The external device requests a memory access at any time by causing the request line, (Erq) to go low. This signal, being low, will set the request detector flip-flop Zx.

$$sZx = Erq\ T7$$

If higher priority I/O channels are not requesting a memory access at the same time, Zx, being true, will initiate a memory access and reset at the following T7 pulse (provided the request signal has been removed)

$$rZx = \overline{Erq}\ T7$$

If, however, a higher priority I/O channel is requesting a memory access, the priority control term Zp1b will be true and Zx will be reset immediately.

$$rZx = Zp1b\ T5$$

If access to memory is made, Zx remains set after pulse time T5 and the MIC signals the external device via (Zad) that access is being made. While (Zad) is true, the device must keep the address lines, (Ia0) through (Ia14), stable. These address lines are inverted in the MIC; thus, the ones complement of the address impressed on these lines will be actually accessed. The request line, (Zrq), must remain active (low) until the MIC acknowledges the request by generating the (Zad) signal.

$$(Zad) = Zx\ (T4 - T0)$$

When accessing memory, the external device or system must notify the MIC whether an input or an output is to take place. The device makes (Z0) true when storing a word in memory and makes (Z0) false when extracting a word from memory. The term Z0 is used to set flip-flop Z9 which enables either (Zdo) (for output) or (Zdi) (for input).

$$sZ9 = Z0\ Zx\ T4$$

$$rZ9 = \overline{Z0}\ \overline{Zx}\ T4$$

$$(Zdo) = Z9\ (T8 - T4)$$

$$(Zdi) = \overline{Z9}\ Zx\ (T2 - Tp)$$

The last two signals advise the external device when output data may be strobed or when input data is being strobed by the computer. The data lines must remain stable while either (Zdo) or (Zdi) is positive.

If the request line (Erq) remains active (low) after transferring a word into or out of memory, the external device may repeat the process with another word by switching to new data, and to another address if necessary. The address lines should be changed only when (Zad) is low. Also, the input and output operations may be interlaced by switching the I/O select signal (Z0). Information transfer rate can be one word per computer cycle (1.75 μsec).

During an input operation the external device supplies data lines, (Zi0) through (Zi23), and the parity bit (Zip). These lines are inverted in the MIC, thus the ones complement of the data impressed on them will actually be transferred to memory. See figure 3-9.

The MIC checks each input word received and reports an error to the device when a word does not have odd parity. The parity error signal line is (Zpe).

$$(Zpe) = (Error)\ (T1 - T7)$$

The MIC provides the even parity bit for each word sent to memory.

During output operations, the external device should strobe the MIC output data lines, (M0z) through (M23z), and the parity bit (Mpz) while (Zdo) is positive. See figure 3-10.

The MIC provides an odd parity bit for each word sent to the external device. It also checks each word received from memory and reports an error to the computer if a word does not have even parity.

DATA MULTIPLEXING SYSTEM (DMS)

Each data multiplexing system consists of a Data Multiplexing Channel (DMC) and one or more Data Subchannels (DSC). The DMC provides service functions for the subchannels and does not connect directly to external units. Memory parity is generated or checked by the DMC for each memory transfer. Each DMC contains a data register, a storage register, and control logic for providing the following functions for associated subchannels:

a. External Addresses. The DMC allows input/output operations to be performed using externally supplied addresses. These operations input to and output from memory locations specified by the device.

b. Internal interlace. With internal interlace, the subchannel supplies the address of an interlace word located in memory. The DMC reads out the contents of this interlace word, increments the address portion, decrements the count, and restores

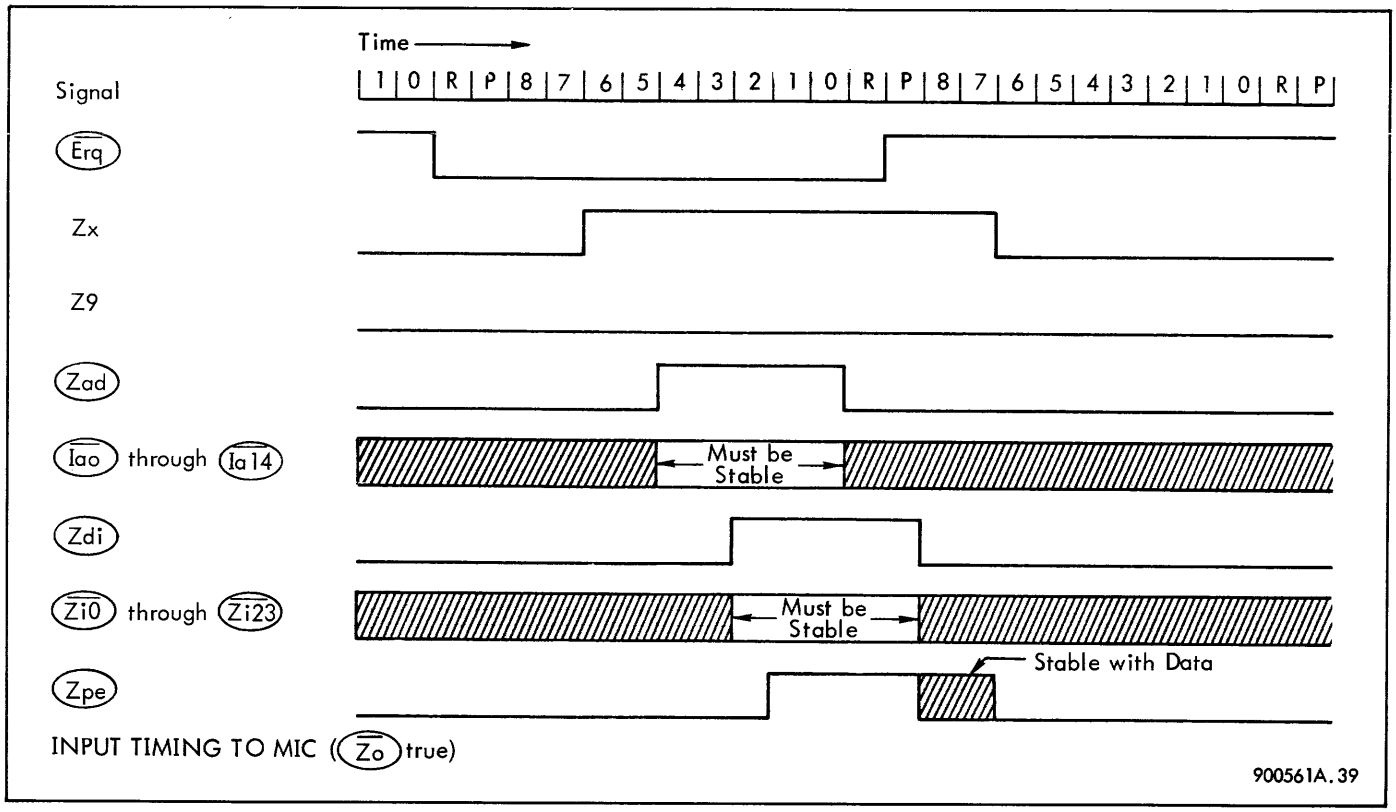


Figure 3-9. MIC Input Timing ($\overline{Zo}$ True)

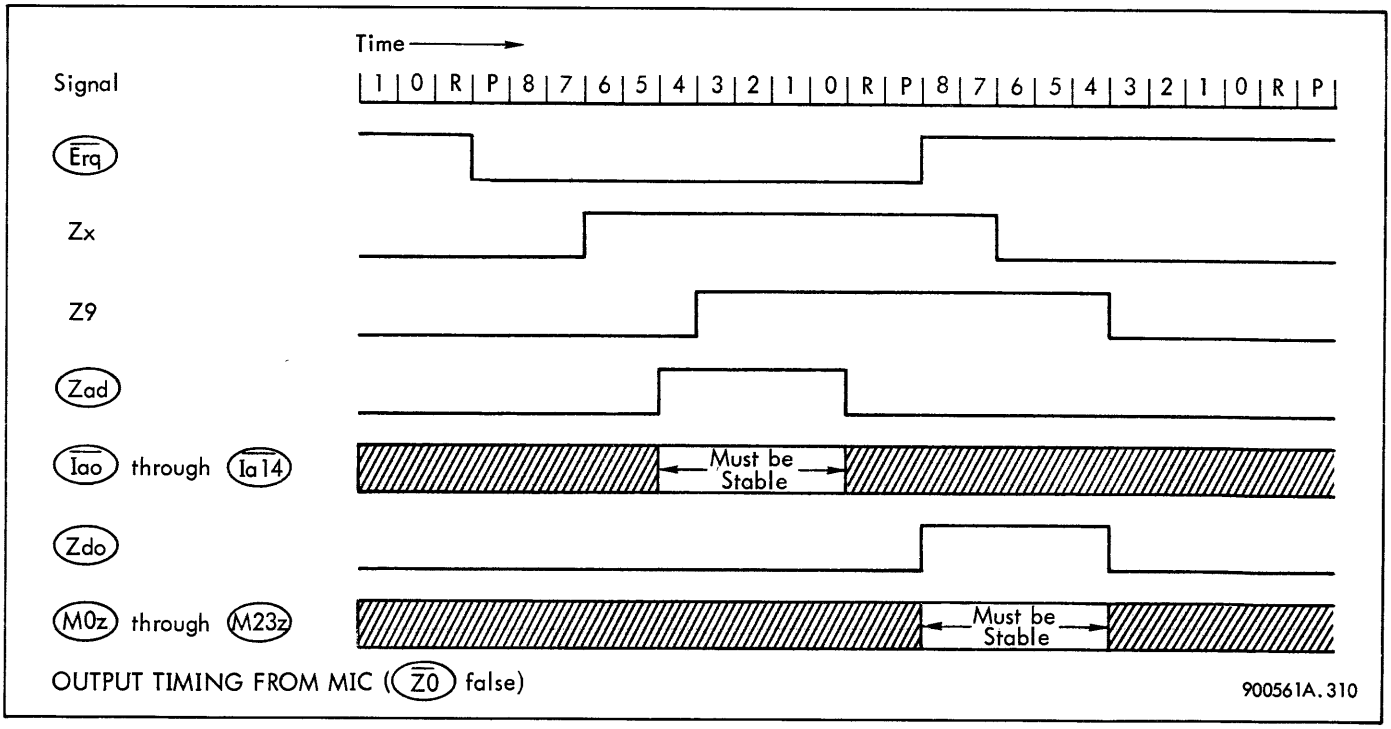
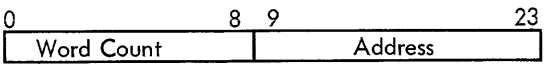


Figure 3-10. MIC Output Timing ($\overline{Zo}$ False)

the updated word to memory. This type of interlace operation requires three cycle times. The format of the internal interlace word is:



c. Automatic memory incrementing. With this feature the subchannel signals the DMC with a word increment code and supplies the address of the word to be incremented. The DMC reads out the word, increments it, and then restores the word to memory. If the word is zero after incrementing, the DMC signals the external unit attached to the DSC which may then interrupt the computer program.

A request for memory access by a DMC is time-shared with other I/O channels connected to the multiple access to memory unit. The manner in which the DMC is interconnected with these I/O channels establishes its priority during the time-shared operation.

Data Subchannel (DSC)

The DSC provides the interface connections between the data multiplexing system and external equipment. Up to 128 DSC's can be connected to a DMC. The subchannels use a priority scheme to determine which may communicate with the DMC at any given time. Subchannels can arm and generate program interrupts, but do not include the interrupt levels themselves. The signal must be routed to optional interrupt levels if the interrupt features are to be used.

A standard DSC using internal interlace has two interlace words assigned to it. These two interlace words are located in adjacent even-odd locations and are fixed for a given subchannel. The program can select either the even or odd location. If the even location is selected, the standard subchannel automatically switches to the odd location when the count field of the even word reaches zero. The program can also select whether or not the subchannel will switch back to the even word when the count field of the odd word reaches zero. The subchannel will generate an interrupt signal when the count field of either word reaches zero. Transmission terminates when the odd word's count equals zero if the subchannel is not instructed to switch back to the even word.

The two-word internal interlace allows a subchannel to handle continuous data by alternately working from one memory area or another. By allowing the subchannel to switch automatically from one interlace word to the other, the program is relieved of the necessity of making real-time responses to the zero count condition. Using first the even then the odd interlace word allows a maximum word count of 1024 for a pair of interlace words.

A DSC can use the internal interlace feature of the DMC to control its transmission, or it can be equipped with an External Interlace (EIN). The EIN consists of a 15-bit address register and a 9-bit count register. When the subchannel is activated, the registers are loaded automatically with the information coming from the internal interlace memory locations. Once the EIN is setup, it controls the transmissions of the DSC at a maximum rate of one word per memory cycle. After each word is transmitted, the EIN adds one to its address register and subtracts one from its count. When the count equals zero, the EIN signals the DSC, which can then generate a program interrupt and/or notify the external unit. Sequencing of interlace words is identical to the sequencing operation performed for internal interlace, except that only two memory cycles are used for interlace word processing. The first is to access the interlace word initially; the second is to restore the interlace word when the word count reaches zero.

Two standard subchannels can be attached to a DMC. The first subchannel (DSC-I) provides an interface that is compatible with standard SDS peripherals. The DSC-I contains a 12-bit character register that can assemble and disassemble two 6-bit characters, and transmit one or two 6-bit characters or one 12-bit character. It checks and generates parity.

The second standard subchannel (DSC-II) is designed to communicate with word oriented input/output units. The external unit must be capable of holding the 24-bit data word during transmission to/from the DMC since the DSC-II contains no storage for data.

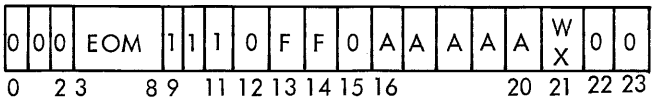
DSC-I Operation

Information pertaining to the operation of the Data Subchannel DSC-I is not available for inclusion in this manual at the time of writing.

DSC-II Operation

Each DSC-II chassis consists of one DSC-II channel (W), or two DSC-II channels (W and X). Because these two channels are identical in their operation, only channel W will be described.

Prior to input/output operations the DSC-II must be selected under program control and placed in the desired mode of operation. The EOM, Internal System Mode (EOM 7) instructions selects and alerts the DSC-II for subsequent operations:



Bit Position	Function
16 through 23	DSC Selection Address, bit 21 is always ZERO for X channel and ONE for W channel. Bits 22 and 23 are always zeros.
13, 14	DMC/DSC function indicators
	00 Activate DSC and device (Buc), or prepare SKS.
	01 Alert channel or external unit for control or test. (Ioc).
	10 Alert channel for interlace control.

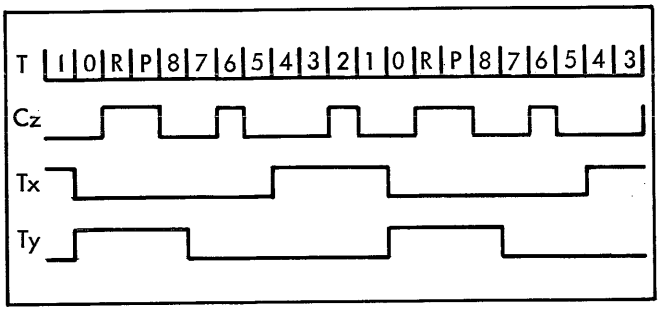
The EOM is followed by a POT or SKS instruction. The function of the POT instruction depends on the previous EOM function indicator bits 13 and 14. Table 3-5 lists the possible EOM/POT or EOM/SKS combinations. The POT interface connectors are not available on the DSC units, therefore the external unit must connect to the TMCC or DACC units for examining the C register outputs during selection or test operations. Once operating parameters have been established, the DSC-II is ready to accept requests from an external device.

Table 3-5. EOM/POT/SKS Function Combinations

Instruction	Interface Term Generated by DSC	EOM Function Indicator Bits	Function
EOM-7 ($\overline{C1}$ C9 C10 C11)		$\overline{C13}$ $\overline{C14}$	1) Select and alert DSC and external unit to examine following POT instruction for control.
POT	Wbuc		1) C19 + C20 + C21 + C22 + C23 activates DSC. 2) $\overline{C19}$ $\overline{C20}$ $\overline{C21}$ $\overline{C22}$ $\overline{C23}$ halts DSC. 3) External unit examines C12 through C23 for selection and control during Wbuc time.
EOM-7 $\overline{C1}$ C9 C10 C11		$\overline{C13}$ $\overline{C14}$	1) Select and alert DSC to accept the following SKS instruction and response.
SKS-7 ($\overline{C1}$ C9 C10 C11)			1) C12 $\overline{C19}$ $\overline{C20}$ $\overline{C21}$ $\overline{C22}$ $\overline{C23}$ tests alerted DSC for being active. 2) External unit examines C12 through C23 for selection and supplies status indication via $\overline{Wssc}$.
EOM-7 ($\overline{C1}$ C9 C10 C11)		$\overline{C13}$ C14	1) Selects and alerts DSC to examine following POT instruction for control. 2) Alerts external unit to examine following POT instruction for control.
POT	Wioc		1) C16 $\overline{C19}$ $\overline{C20}$ $\overline{C21}$ $\overline{C22}$ $\overline{C23}$ resets cycle flip-flop in alerted DSC.
EOM-7 ($\overline{C1}$ C9 C10 C11)		C13 $\overline{C14}$	1) Selects and alerts DSC to examine following POT instruction for interlace control.
POT			1) C20 arms end-of-record interrupt. 2) C21 arms word-count-equals-zero interrupt. 3) C22 sets cycle flip-flop. 4) C23 sets even/odd flip-flop. The interlace word address will be odd.

Basic DMC/DSC Training Pulses

Computer timing is not used directly in the DSC's; timing signals on the POT connector (Qq1, Qq2 and Qq3) should not be used. The DMC generates timing pulses internally for use by the DSC's and by the input/output devices. These three pulses are illustrated below.



The Cz pulse is a clock generated in the DMC for use by the DSC's. Tx and Ty timing pulses are made available for use by external devices. The computer timing pulses are not available to the DSC's or to the external devices.

Request Line Considerations

When a selected device wishes to input, output, or increment a word, it must provide a request signal (Wsrq) to the enabled DSC-II ((Wsrq) at 0v). When the DSC-II recognizes a request it sends a (Wrq) signal to the external unit so it will know that its request has been acknowledged.

$$sWrq = Wsrq\ Wac\ \overline{Wh}\ Ty$$

For medium speeds the device may enable (Wsrq) when (Wrq) is off, and then remove (Wsrq) when (Wrq) comes on. At high speeds, however, (Wrq) may remain on continuously from one word to the next. In this case the device can use Wx Zad as an indication that each request has been processed. If (Wsrq) is removed on the occurrance of Wx Zad, however, the subchannel will already be in the process of responding to one more request.

In this case the device may remove the request after a desired time period, or it may keep track of the number of requests which have been completed by counting Wx Zad signals. In counting Wx Zad the device must remove its request in time to allow Wrq to be reset by the next Ty Cz clock; otherwise another request will be made.

High speed operations can be terminated by the external unit if a halt signal (Whs) is generated while (Zad) is true during the transmission of the next-to-last character. See figure 3-11. The halt detect flip-flop will be set at the trailing edge of (Zad).

$$sWh = Wac\ Whs\ Tx$$

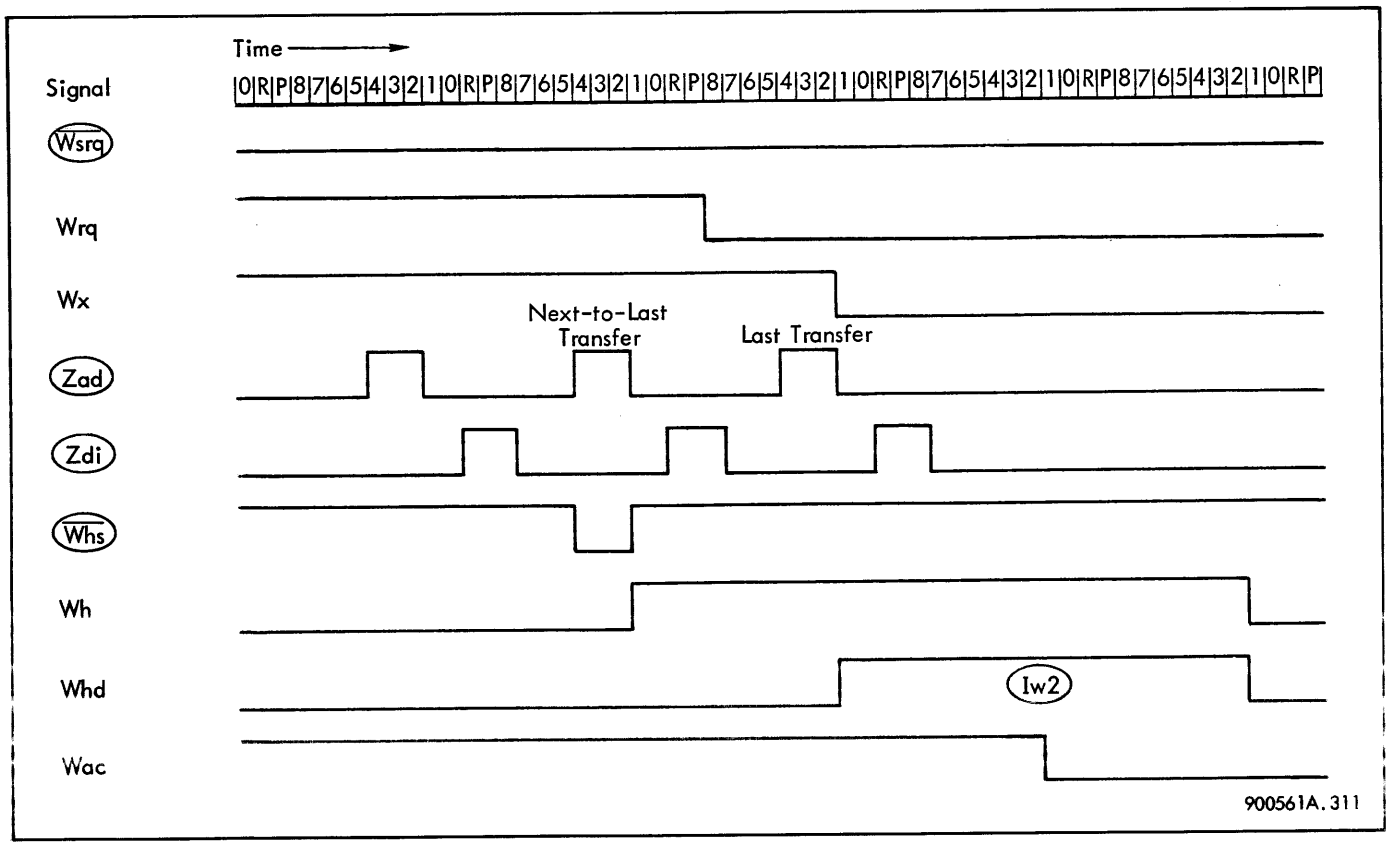


Figure 3-11. Timing Diagram DSC-II Terminating Input/Output with External Address

Since the term Wh is part of the request detect flip-flop logic, further requests by the external unit are not accepted.

$$sWrq = Wsrq\ \overline{Wh}\ Ty\ Wac$$

After the DSC has transferred the last character, the W-active flip-flop will be reset.

$$Whd = Wh\ \overline{Wrq}\ \overline{Wx}\ \overline{Ewrq}\ \overline{Ewx}$$

The terms $\overline{Ewrq}$ and $\overline{Ewx}$ pertain to requests from the external interface option and may be assumed true for this discussion.

$$rWac = Whd\ Tx$$

Input Using External Address

When ready to access memory, the external unit supplies a ground to request line (Wsrq). This condition sets request detect flip-flop Wrq. See figure 3-12.

$$sWrq = Wsrq\ Wac\ \overline{Wh}\ Ty$$

For inputs using external addressing, all function code lines are high (logical zero). See table 3-6. The memory address lines (Wa0) through (Wa14) must be stable while Wx is true. A logical ONE is represented by a ground level on these lines. The request select flip-flop, Wx, will set provided there are no requests being processed by higher priority channels.

$$sWx = Wrq\ \overline{Ewrq}\ \overline{Ewx}\ \overline{Srqx}\ (Srq + Zad)\ Tx$$

Request detect flip-flop, Wrq, will now reset provided the set signal is removed.

$$rWrq = Wx\ Ty + Wh$$

The term (Zad) is now supplied by the DMC signifying that the request is being processed. This term is true during Tx. Flip-flop Wx is reset at the end of (Zad) is a new request is not being made.

$$rWx = Zad + - - -$$

The trailing edge of (Zad) also indicates that the address lines may be changed. The input data lines (Wd0) through (Wd23) and (Wdp) must be held stable until the term (Zdi) is supplied by the DMC. The input lines may be changed after (Zdi) has returned to the false state. A logical ONE is represented by a ground on the data lines (Wd0) through (Wd23) and (Wdp). The external unit should not accept (Zdi) signal until after receiving (Zad) with (Wx) true. The (Win) signal supplied by the DSC is used to gate (Zdi) at the external device.

$$sWin = Zad\ Wx$$

$$rWin = Zad$$

The DMC checks each input data word for odd parity. If an error is detected, the interface signal (Zpe) is generated. This signal may be strobed when (Zdi) (Win) is true.

Table 3-6. Relationship of DMC Functions and Interface Signals

Subchannel Function Code Lines			DMC Function	DMC Response	Number of Machine Cycles
$\overline{Wf1}$	$\overline{Wf2}$	$\overline{Wf3}$			
0	0	0	Store a Word in Memory	Zad, Zdi	1
0	0	1	Access a Word from Memory	Zad, Zdout	1
0	1	0	Store a Word in Memory using Internal Interlace	Zad, Zdi	3
0	1	1	Access a Word from Memory using Internal Interlace	Zad, Zdout	3
1	0	0			
1	0	1	Increment a Word in Memory (Low Order 12 Bits Only)	Zad, Zdi	2
1	1	0	Increment a Word in Memory (High Order 12 Bits Only)	Zad, Zdi	2
1	1	1	Increment a Word in Memory (Entire Word)	Zad, Zdi	2

Logical ONE on the Function Code lines is represented by zero volts.

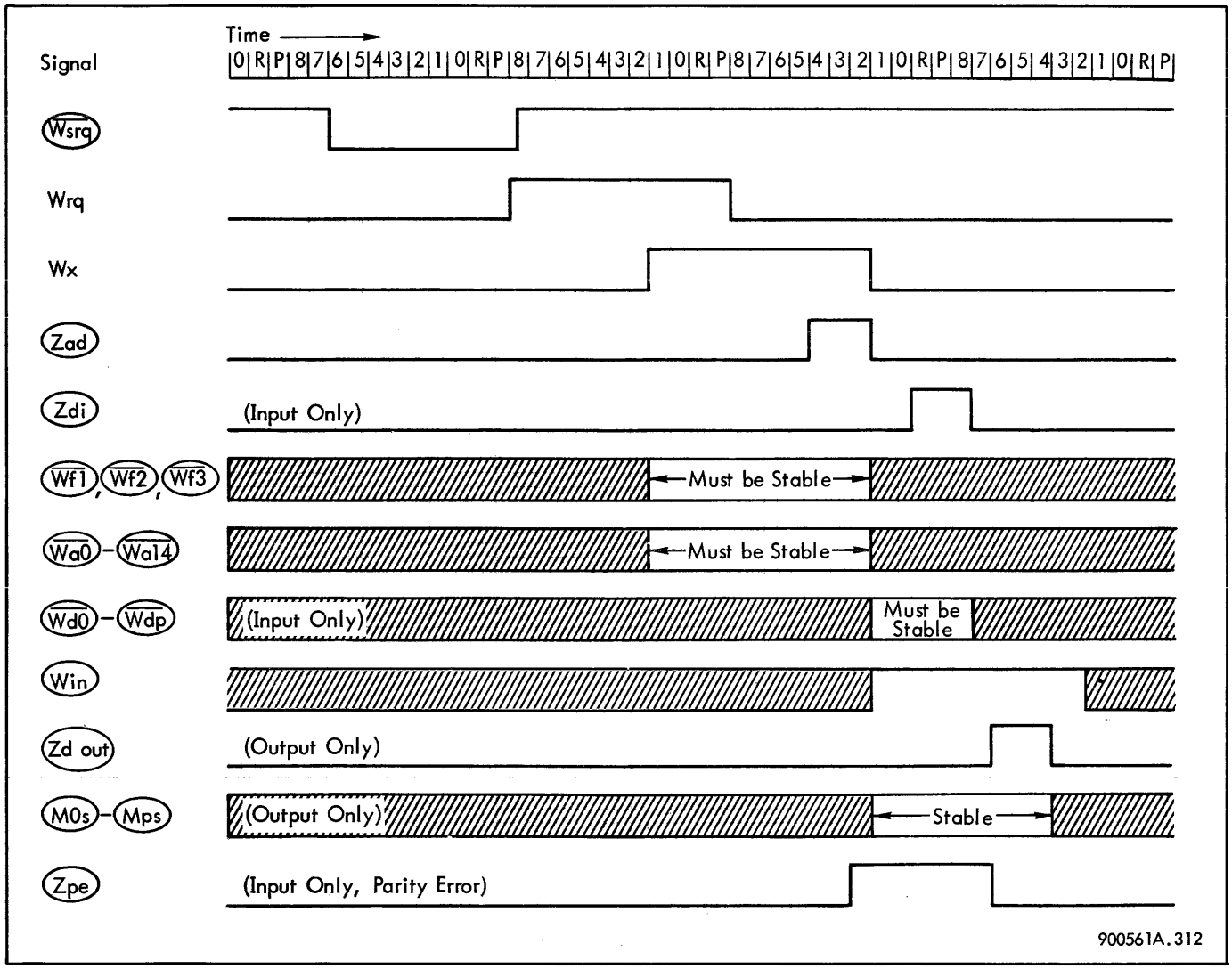


Figure 3-12. Timing Diagram DSC-II Terminating Input/Output with External Address

Output Using External Address

An output operation is identical to the input operation with the following exceptions:

a. The external unit must supply function codes: $\overline{Wf1}$ high, $\overline{Wf2}$ high, and $\overline{Wf3}$ low.

b. The DMC generates the term Zdout to inform the external unit that the data output terms M0s through M23s and Mps are stable and should be strobed.

The Zdout term must not be accepted until Win comes true. See figure 3-12.

Input/Output Using Internal Interlace

When the internal interlace feature is used, interface signals are identical to those previously described with the following exceptions: see figure 3-13.

a. The external unit must supply the function code corresponding to interlace operation.

b. The maximum data transfer rate is one word every three cycles. The extra cycles are required by the DMC for updating the interlace word and restoring it to memory.

c. Address information for interlace functions is supplied by the DSC-II. This address is generated by a prewired jumper module and serves to locate the selected channel's interlace word in memory.

Although the term that indicates the interlace word equals zero, Zdz, is available at the interface connector, it should not be used for this purpose since this term will not be generated if the external interlace feature is used.

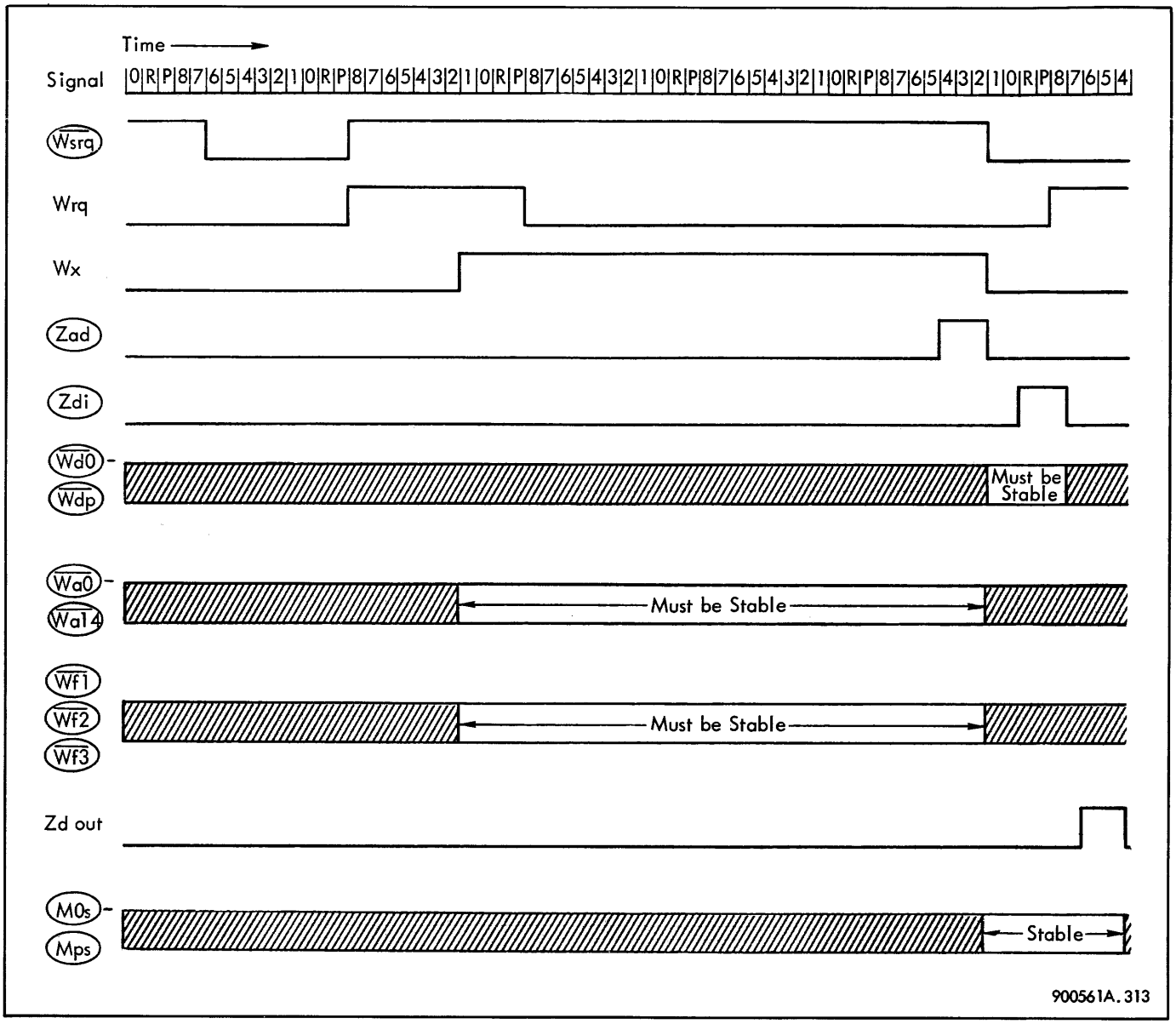


Figure 3-13. Timing Diagram DSC-II Input/Output Using Internal Interlace

Input/Output Using External Interlace

When interlace operation is required at a higher data transfer rate than can be obtained by using internal interlace, an external interlace unit can be connected to the DSC-II. The external interlace unit contains a 15-bit address register, 9-bit word-count register, and counter logic for performing the interlace word updating at a rate of one word every cycle. Programming considerations for external interlace are identical to those for internal interlace. The interlace word is transferred from the memory location to the external interlace register during the normal EOM/POT sequence for setting up the interlace parameters. Before supplying a terminating interrupt when the word count equals zero, the updated interlace word is restored into its preassigned memory location.

The external unit receives and supplies interface signals identical to those for internal interlace except at a higher rate.

The terms (Zad) and (Zdi) occur during loading and restoring the interlace word and must be ignored by the external unit. This can be accomplished if (Zad) is always gated with (Wx), and if (Zdi) is always gated with (Win).

Word Increment Function

The external unit can request a word increment function by holding function code line (Wf1) low during an access request. The memory address of the word to be incremented is also supplied by the external unit. See figure 3-14.

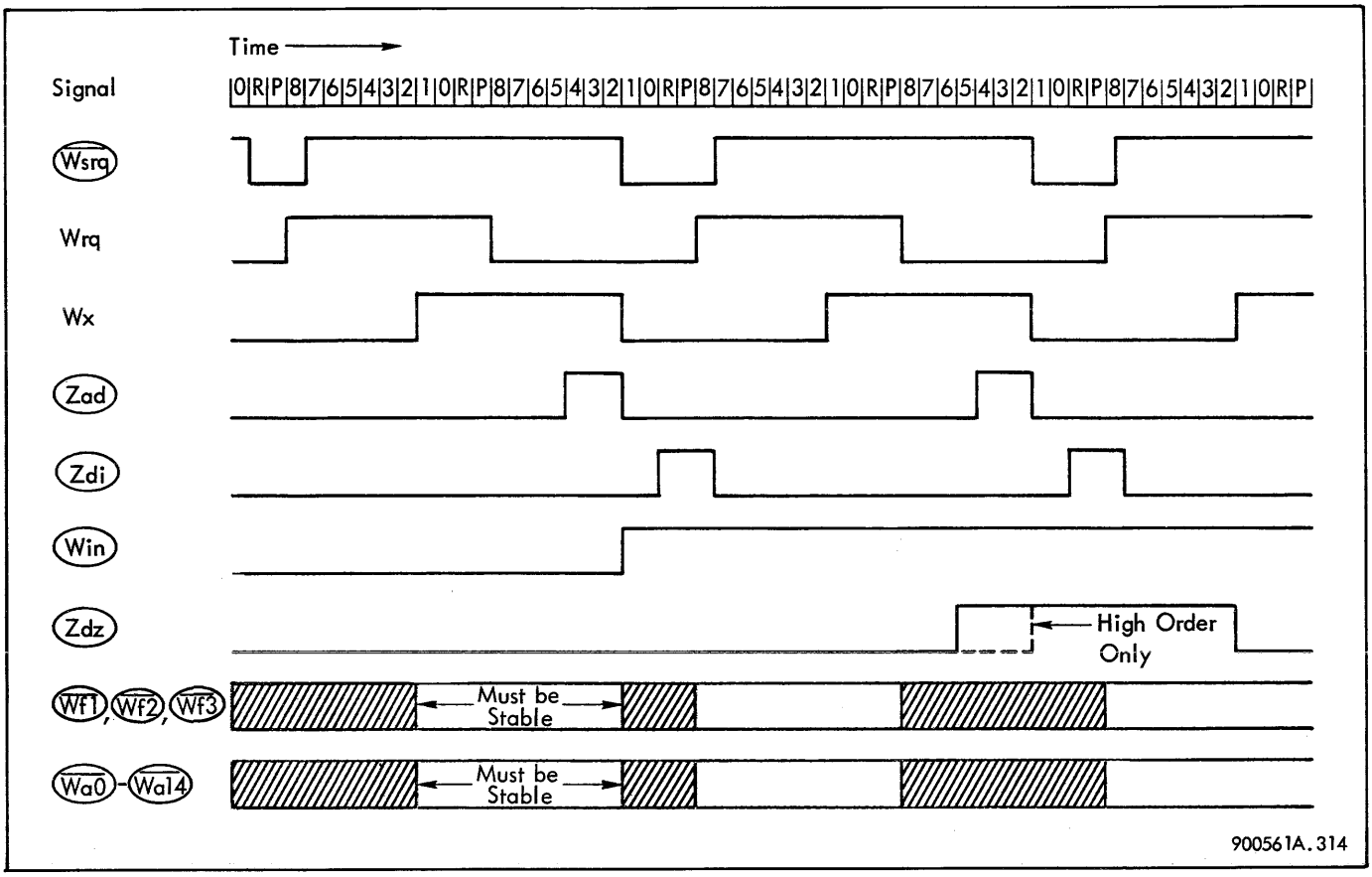


Figure 3-14. Timing Diagram DSC-II Word Increment Function

Function code lines (Wf2) and (Wf3) determine whether a partial or full word is incremented. The interface signal sequence and timing is similar to that of externally addressed inputs. The maximum increment rate is one word every two cycles.

When the contents of the incremented word reach zero, the DMC will generate a (Zdz) signal which may be strobed by the external unit when (Zdi) is true. Only the portion of the word that was actually incremented will be examined by the DMC to determine the all-zero condition. This increment function can be terminated in the same manner as the externally addressed I/O either by an EOM/POT instruction sequence which sets the halt detect flip-flop, Wh, or by the external unit supplying the halt signal, (Whs).

PRIORITY INTERRUPT OPERATION

The 925/930/9300 priority interrupt system provides up to 896 general purpose priority interrupt channels for external system use. Each interrupt channel has a unique memory location assigned to it. These memory locations are numbered in octal sequence from 00200 in the 925/930 and from 00040 in the 9300. Interrupt channels have priority according to memory location number. Priority is inversely proportional to the memory location number; that is, memory location 200 has priority over memory location 201.

An incoming interrupt signal, generated by the external system, is examined by internal logic and causes the computer to interrupt the program sequence at the completion of the current instruction execution. A transfer of program control is forced by the interrupt logic to a preassigned interrupt memory location without disturbing the program counter. A mark place and branch instruction (BRM) in this location saves the contents of the program counter, the overflow indicator, and the memory extension register bits, and then transfers to the particular interrupt service routine required. Since each interrupt is associated with a unique memory location the proper service routine is always entered. To exit from the routine, an uncondition branch (BRU) instruction with indirect addressing returns control to the next instruction in proper sequence in the main program. The BRU instruction with indirect addressing always clears the active interrupt.

A "single instruction interrupt" causes the execution of only one instruction before automatically clearing itself and returning to the program that is interrupted. No branch instruction is needed to clear the interrupt. Any of the optional general purpose interrupts can be single or normal instruction interrupts in any combination desired.

Interrupt States

Each interrupt channel has two flip-flops associated with it. These flip-flops indicate the status of the interrupt channel as follows:

Storage Flip-Flop	Process Flip-Flop	Status
0	0	No interrupt received (inactive).
1	0	Interrupt received but not being processed (waiting).
1	1	Interrupt received and being processed (active).
0	1	Nonallowable configuration.

In the inactive state, no interrupt signal has been received by the channel and none is currently being processed by its interrupt servicing routine. In the waiting state, an interrupt has been received by the channel but it is not being processed. This situation may be due to an interrupt of higher priority being processed at this time. When all higher waiting interrupts have been processed, this channel goes to the active state. In the active state the interrupt has been acknowledged, meaning it has caused the main program to recognize its presence and has transferred to its assigned interrupt location where it is being processed.

The single instruction interrupt operates in the same way as the normal priority interrupt in the inactive and waiting states. However, when acknowledged, this interrupt enters the active state and remains there during the execution of one instruction. At the completion of the one instruction, the single instruction interrupt returns to the inactive state without the aid of a branch instruction.

While in the active status, the interrupt channel rejects new stimuli regardless of its duration or the number of times it has occurred.

All interrupt channels are cleared to the inactive state when the start button is depressed.

Individual interrupt channels may be armed or disarmed, or all system channels may be enabled or disabled as a group. Arm/disarm controls the change from the inactive state to the waiting state. The disarm condition of an interrupt channel causes that channel to retain no record of an interrupt signal entering the channel. Enable/disable controls the change from the waiting to the active state. When enabled, an interrupt proceeds from the waiting state to the active state as soon as its priority allows. When disabled, an interrupt remains in the waiting state until enabled.

Interface Signals

Each general purpose interrupt channel has a unique interrupt request input line associated with it. These lines are numbered in decimal sequence from (I5) through (I900) . The request line (I5) corresponds to memory location 00200 in the 925/930 and 00040 in the 9300. The quiescent condition of these lines is false.

The interrupt request line is activated by the external device associated with it. The storage flip-flop of the channel detects the presence of an interrupt request signal. This flip-flop strobes the input line once every computer cycle at T1 time. The interrupt request signal from the external device must therefore be true for a minimum of one machine cycle (1.75 μsec) to ensure acknowledgement by the storage flip-flop. The interrupt request signal must return to its quiescent state (false) before the completion of the interrupt servicing routine, otherwise double interruption will occur. Figure 3-15 describes the total system priority interrupt capability.

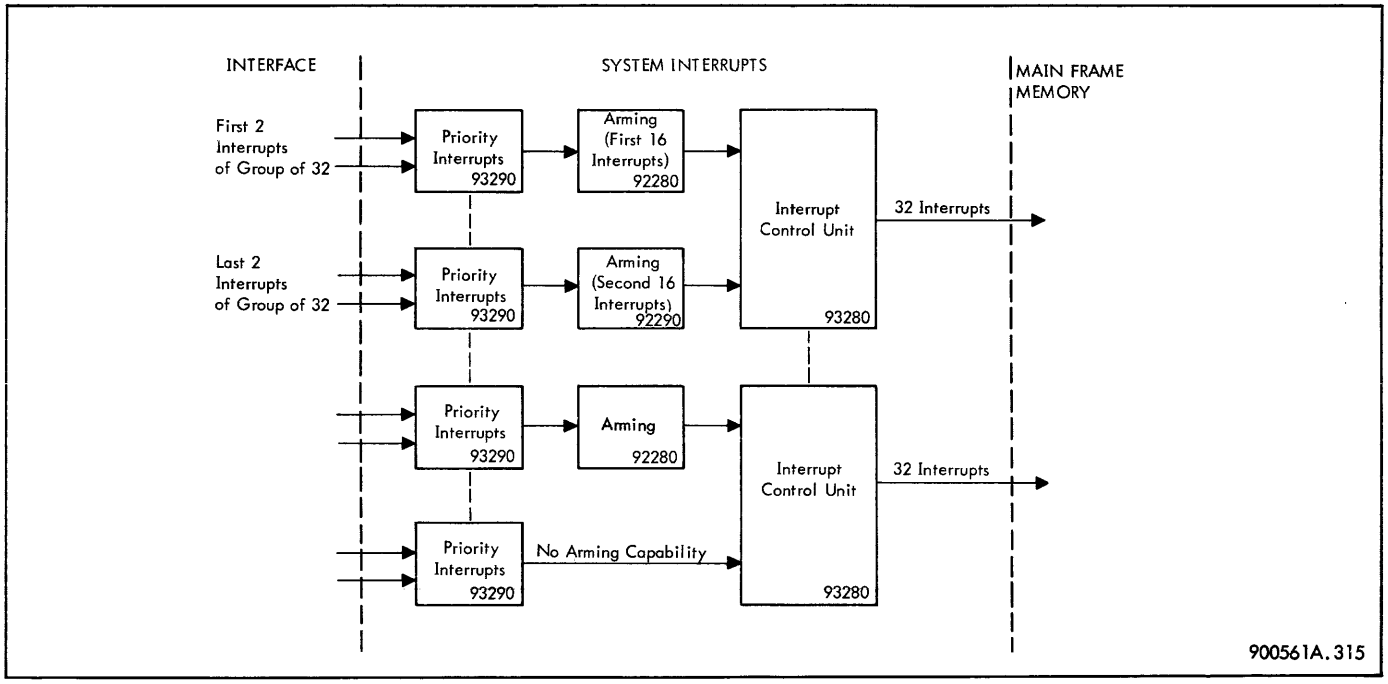


Figure 3-15. System Priority Interrupt Configuration

SECTION IV INTERFACE CIRCUIT AND CABLE REQUIREMENTS

GENERAL

This section provides interface circuit and cable descriptions necessary to connect the external equipment to the SDS 925/930/9300 Computers input/output systems.

The following definitions are used in the description of the I/O circuits:

a. Unit Load: A unit load is defined as 3 ma to the driving source at the 0v level, and no current at the 8v level. A typical AND gate with one unit load is illustrated in figure 4-1.

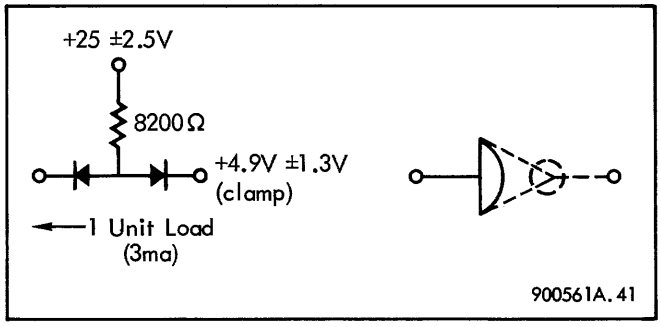


Figure 4-1. Typical AND Gate

b. Input Logic Levels

Binary ONE (True) +6v to +20v (nominal +8v)

Binary ZERO (False) -2v to +2v (nominal 0v)

c. Output Logic Levels

Binary ONE (True) +6.5v to +9.5v (nominal +8v)

Binary ZERO (False) 0v to +0.8v (nominal 0v)

CABLE REQUIREMENTS

In all cases shielded cable should be used. The preferred cables are specified in SDS drawings as follows:

a. 101932 Single Shielded Cable

b. 101787 14-Conductor Cable (Individually Shielded)

c. 102872 30-Conductor Cable (Individually Shielded)

These cables have the following approximate characteristics:

Inductance:	50 nh/ft
Capacitance:	50 pf/ft
Impedance:	33 ohms
Resistance of Center Conductor:	23 milliohms/ft
Resistance of Shield:	10 milliohms/ft

CONNECTOR REQUIREMENTS

All input/output connectors are 47-pin ELCO Varicons. The recommended mating cable plug modules are: (1) SDS Model ZX13 for low-speed signal transmission, and (2) SDS Model ZX34 for high-speed signal transmission.

The printed wiring arrangement of the ZX13 and the ZX34 permits the mounting of both series components and/or pull-up resistors on each signal line.

CIRCUIT REQUIREMENTS

The I/O system provides several types of cable driving/receiving combinations. In the description of the following interface signals, each signal driver/receiver is classified as follows:

Ox = Output
Ix = Input

The "x" term represents an arbitrary number to subdivide the input or output groups.

OUTPUT CIRCUITS

Most outputs require either cable driver AK53 or cable driver AK56, depending upon the output speed requirements.

Low-Speed Outputs, Type 01

For this type of output the cable driver AK53 is used. Its output stage and logic diagram are shown in figure 4-2.

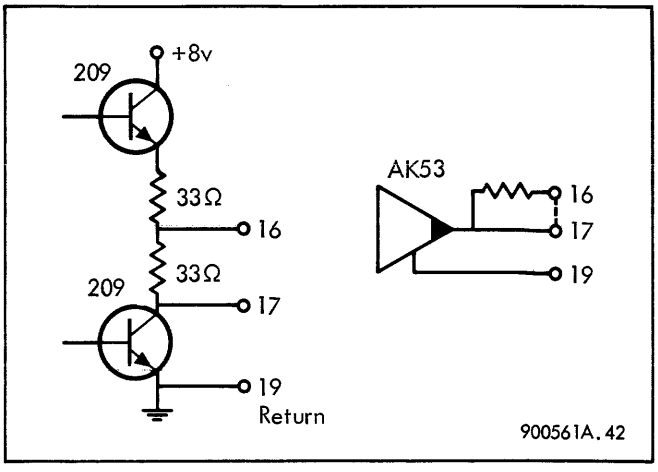


Figure 4-2. Cable Driver AK53

In all cases, terminals 16 and 17 (or the corresponding terminals of other circuits) are connected together. The output can be shorted to ground without damaging the circuit. The method of connecting to the output is by a parallel inductor-resistor circuit. A typical interface connection is shown in figure 4-3.

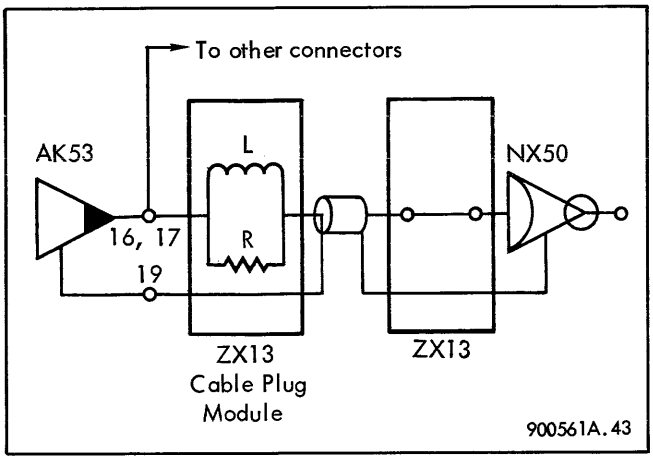


Figure 4-3. Typical Interface Connection, Low-Speed Outputs, Type O1

Circuit characteristics (with pins 16 and 17 connected together) are as follows:

Output Impedance (True State)	33 ohms (to +8v)
Output Impedance (False State)	3 ohms (to gnd)
Drive Capability	91 unit loads
Output Delay (Typical)	70 nsec

The preferred receiver is the NX50 which is described in more detail under input circuits.

The values of the inductor and resistor depend upon the cable length, and the amount of delay, T_D, that can be tolerated. Table 4-1 lists the values of L and R, and the effective load, N, (in unit loads of 3 ma) for delay times that are usable with the SDS 925/930/9300 Computers.

This tabulation assumes that the load at the receiving end of the cable does not exceed N/5. If the number of loads M at the receiving end is greater than N/5, an extra delay, ΔT, will occur, given approximately by the formula:

$$\Delta T = L(M-N/5)\ nS$$

where L is the inductance in microhenries. The resistor should conform to SDS specification 100111, and the inductor should conform to SDS specification 100342. These components should be mounted on a cable plug module type ZX13. The NX50 Interface Inverter is the preferred receiver. Each interface inverter presents a load of two units (6 ma) to the cable driving it.

Table 4-1. R/L Network Values

	T_D = 68 nS			T_D = 100 nS			T_D = 150 nS			T_D = 220 nS			T_{D_1} = 330 nS		
Length (Ft)	L	R	N	L	R	N	L	R	N	L	R	N	L	R	N
4.7	22	220	15	47	330	10	100	470	6.8	220	680	4.7	-	-	-
6.8	15	150	22	33	220	15	68	330	10	150	470	6.8	-	-	-
10	10	100	33	22	150	22	47	220	15	100	330	10	220	470	6.8
15	6.8	68	47	15	100	33	33	150	22	68	220	15	150	330	10
22	4.7	47	68	10	68	47	22	100	33	47	150	22	100	220	15
33	-	-	-	6.8	47	68	15	68	47	33	100	33	68	150	22
47	-	-	-	-	-	-	10	47	68	22	68	47	47	100	33
68	-	-	-	-	-	-	-	-	-	15	47	68	33	68	47
100	-	-	-	-	-	-	-	-	-	-	-	-	22	47	68

L in microhenries

R in ohms

N in unit loads of 3 ma

Low-Speed Outputs, Circuit Type 02

Some input/output channels use the Cable Driver Module AK57 for low-speed outputs. Figure 4-4 shows the basic output stage and the logic diagram

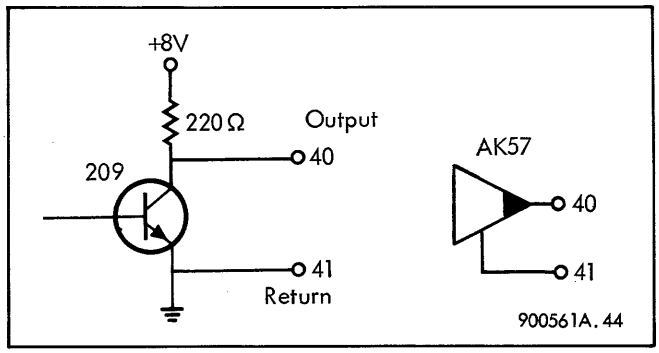


Figure 4-4. Cable Driver AK57 Output

This module contains 16 circuits. Ground returns are provided for circuit pairs and should be connected to ground at a point near load circuits. This driver is intended primarily for driving lines with parallel inductor-resistor networks in series with the load. The output driving capability when false (output transistor "on") is 60-unit loads. Output drive capability is limited by the 220-ohm collector resistor when the output is true (output transistor "off"). If a part rise time is required, the receiving end of the driven line may be terminated with a pull-up resistor. See figure 4-5.

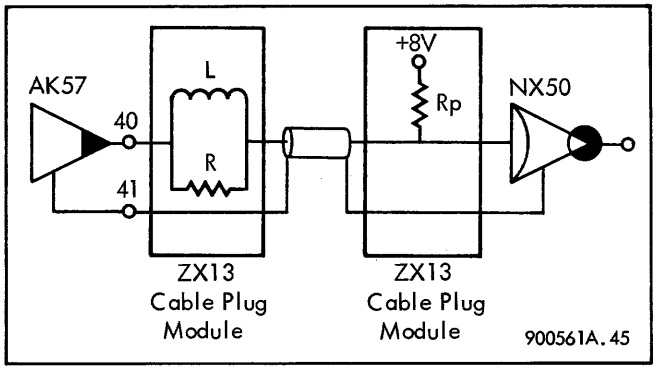


Figure 4-5. Low-Speed Output, Circuit Type O2

The values of L and R may be chosen from the values suggested in table 4-1. The value of Rp should be equal to R in the RL network.

Circuit characteristics are as follows:

Output Impedance (True State)	220 ohms (to +8v)
Output Impedance (False State)	3 ohms (to gnd)
Drive Capability	60 unit loads
Output Delay (Typical)	80 nsec

High-Speed Outputs, Circuit Type 03

Some outputs make use of the high-speed, low-impedance, cable driver type AK56. Its output stage and logic diagram is shown in figure 4-6.

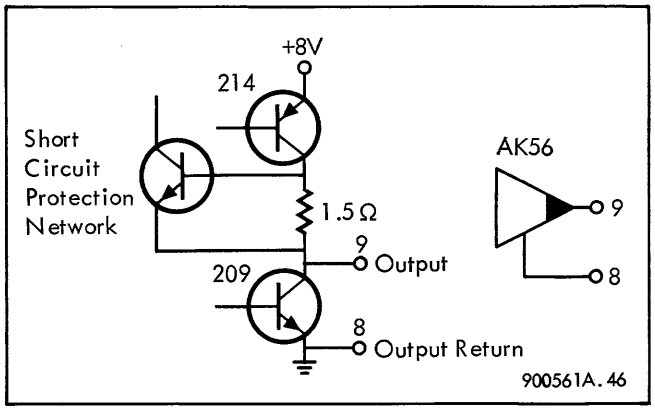


Figure 4-6. Cable Driver AK56

The output of the AK56 is taken from terminal 9 (or the corresponding terminals of other circuits). The output is protected for output shorts to ground. For the DACC's, two types of output connections are possible: one type intended for low-speed output connection identical to those described under Low-Speed Outputs, Circuit Type O2; and another type for high-speed output connections. Both types of outputs may be driven simultaneously, providing the load rating of the AK56 is not exceeded. The high-speed output connection is made through a series resistor of 33 ohms. See figure 4-7. The cable is thus approximately matched at the sending end.

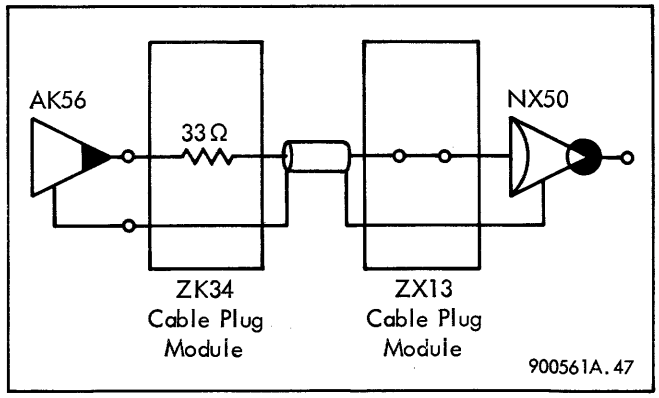


Figure 4-7. High-Speed Output, Circuit Type O3

When the AK56 switches, a wave of 4v amplitude is launched at the cable input. On arrival at the receiving end, it doubles its amplitude by reflecting back a wave of similar amplitude which is then absorbed at the termination. Thus, the time of delay is equal to the time of a single transit down the cable. Not more than 6-unit loads should be connected at the receiver end. The NX50 is the

preferred input circuit. The high-speed configuration presents to the driver a transient load of 40 units, plus the dc load equal to the number of gate loads at the receiving end of the cable.

Circuit characteristics are as follows:

Output Impedance (True State)	4 ohms (to +8v)
Output Impedance (False State)	2 ohms (to gnd)
Drive Capability	120 unit loads
Output Delay (Typical)	60 nsec

The interface Inverter NX50 is the preferred input circuit. The high-speed configuration presents to the driver a transient load of 40 units, plus the dc load equal to the number of gate loads at the receiving end. See figure 4-8.

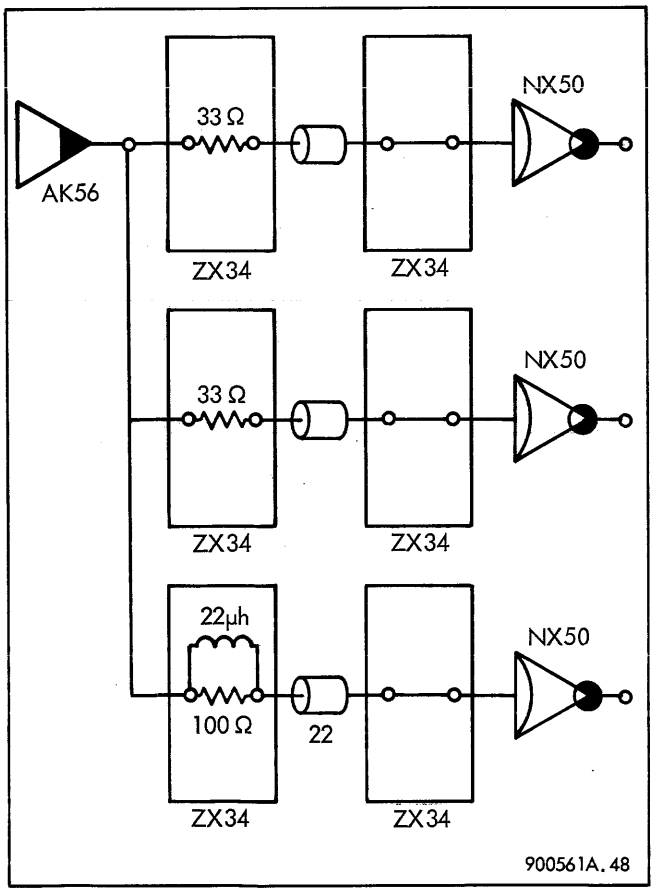


Figure 4-8. Cable Driver AK56 Loading

INPUT CIRCUITS

Most general purpose input circuits for the SDS 925/930/9300 Computers use the Interface Module type NB50 (inverter), or in the case of the DSC channels, the NX50.

Input Circuit Type I1

The input stage and logical diagram for the NB50 Interface Inverter is shown in figure 4-9.

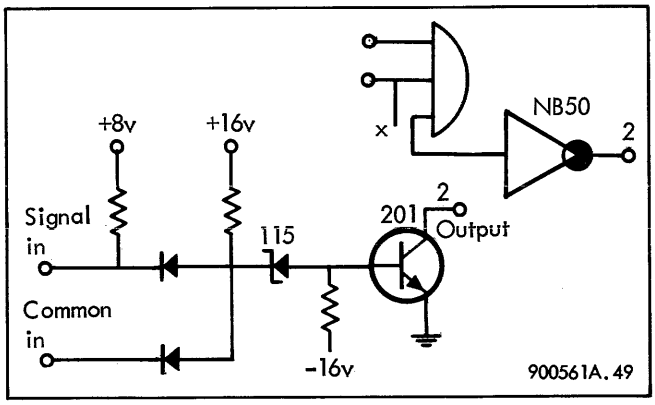


Figure 4-9. Interface Inverter, NB50

The SDS 115 Zener diode at the input to the NB50 circuit rejects input noise. Since, in general, input signals are logically inverted (true = 0v), a positive AND gate may "or" several inverted input terms, if required, as shown in figure 4-10.

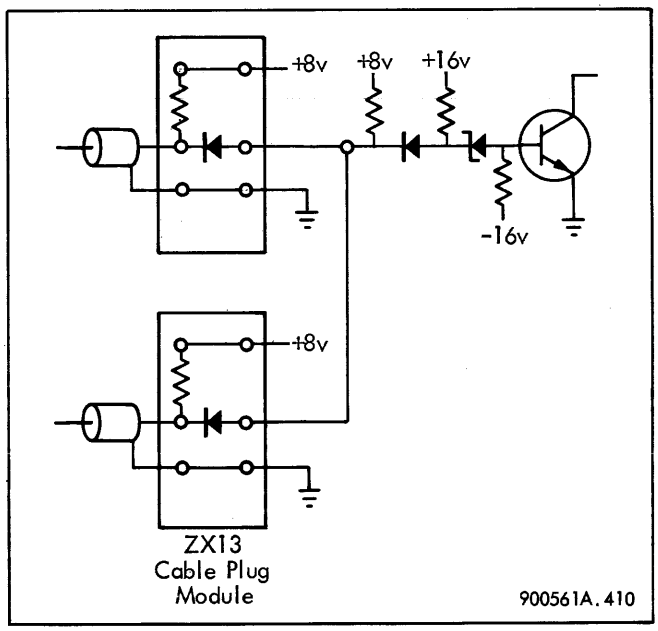


Figure 4-10. Input Signal Gating

Circuit characteristics of the NB50 are:

Gate Input Loading	2 unit loads
Output Delay	50 nsec
Input Threshold	+3.5v (approx.)

The PIN signals are treated as type I1 inputs; however, an additional load is present on the inputs (Cd9) through (Cd23). This load is 500 ohms connected to +8v for each TMCC or DACC rack. There are two TMCC channels in one rack.

Input Circuit Type I2

The Interface Inverter Module NX50 is designated as type I2 input circuit. These modules are used as input receivers in the DSC-I channels, and have identical input characteristics as those of the NB50.

Input Circuit Type I3

Some input circuits must drive the Schmitt Trigger Module AK54. The AK54 presents two unit loads (6 ma) to the driving source. A suggested method of driving the AK54 is shown in figure 4-11.

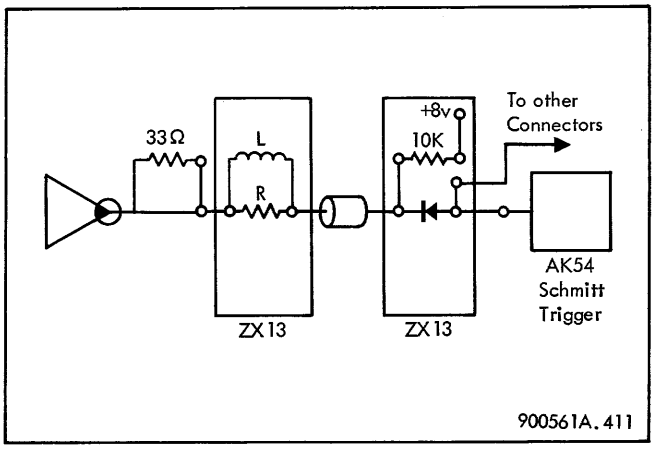


Figure 4-11. Input Circuit Type I3

Input Circuit Type I4

If the arming feature is not present, the input circuits of the interrupt lines are Priority Interrupt Modules SK61. These circuits present a two unit load (6 ma) to the driving source. Each interrupt connector can accept up to 32 input lines. However, to prevent false interrupts, each unused input connector pin must be connected to computer ground. The circuit arrangement for this type of input is shown in figure 4-12.

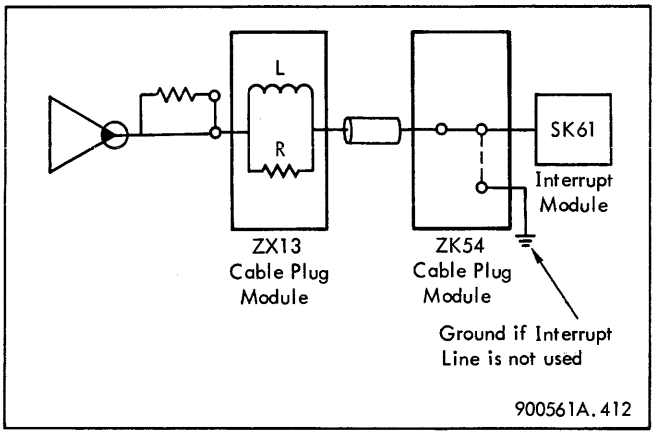


Figure 4-12. Interrupt Inputs Type I4

If the arming feature is present, the input circuits for the interrupt lines are Buffered AND Gate Modules BH12. The interface considerations are identical to those described for the the SK61.

Driving Input Signals

The arrangement for driving low-speed inputs is similar to that for low-speed outputs. The preferred driving circuit is the Cable Driver AX14. Its output is shown in figure 4-13.

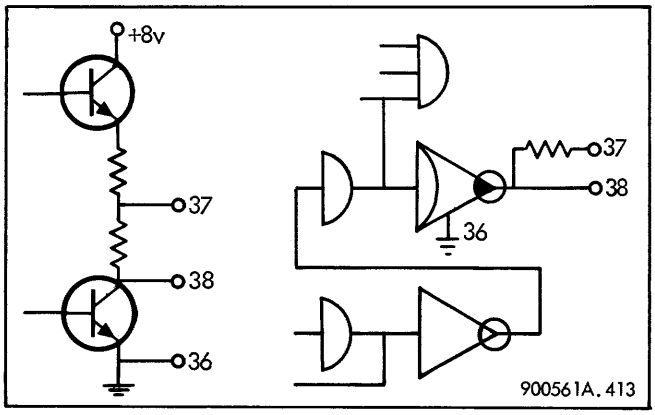


Figure 4-13. Low-Speed Input Cable Driver AX14

There are seven circuits on each AX14 module, plus one common disable input which inhibits all the outputs. The AX14 is capable of driving 75 unit loads. Its output can be shorted to ground without damaging the circuit. For low-speed signals, the cable driver is connected to the computer by the circuit shown in figure 4-14.

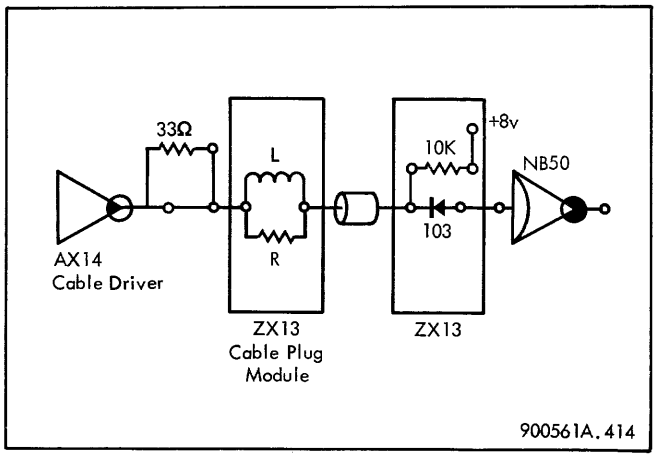


Figure 4-14. AX14 Driving Low-Speed Input

The resistor-inductor circuit is chosen in the same manner as for low-speed outputs. See table 4-1 for correct values. The diode is included to isolate inputs from each other, and the resistor connected to +8 volts ensures that if the AX14 module is disabled, or if its supplies are turned off, the line potential will be maintained at +8 volts.

High-Speed Inputs

The circuit arrangement for high-speed input signals also uses the Cable Driver type AX14 and is shown in figure 4-15.

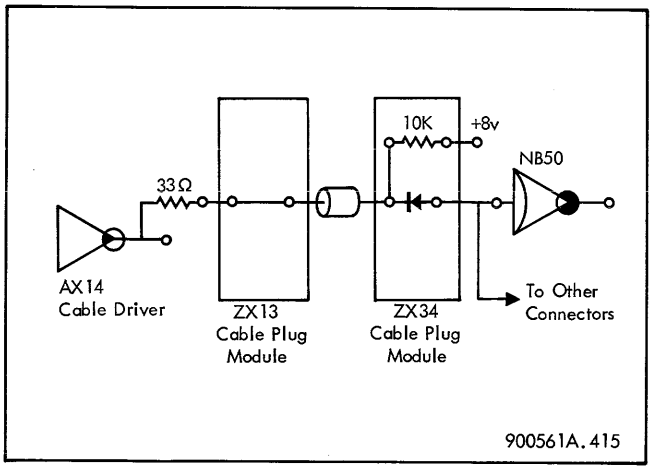
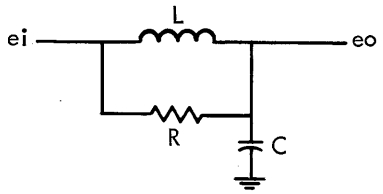


Figure 4-15. High-Speed Input Connection

The resistor connected to +8 volts and the diode fulfill the same function as for low-speed inputs. However it must be mounted on a Cable Plug Module type ZX34 (Input and output signals are mixed on the same module, and the ZX13 is not suitable for high-speed outputs).

FORMULAE FOR LRC CIRCUITS

For the low-speed transmission, the equivalent circuit is



where C is the cable capacity. The transfer function of this circuit is

$$\frac{e_o}{e_i} = \frac{1 + 2Ks}{1 + 2Ks + s^2}$$

where

$$s = p\sqrt{LC}$$

$$K = \frac{1}{2R}\sqrt{\frac{L}{C}}$$

p = Laplace variable

With

$$K = \frac{1}{\sqrt{2}}$$

the output response in normalized time (unit $= \sqrt{LC}$) for a unit step input is

$$e_o = 1 - \left(\cos \frac{t}{\sqrt{2}} - \sin \frac{t}{\sqrt{2}}\right) \frac{t}{\sqrt{2}}$$

$$= 1 \text{ when } \frac{t}{\sqrt{2}} = \frac{\pi}{4}$$

i.e., when $t = 1.1$

The overshoot is

$$\epsilon^{\frac{-\pi}{2}} = 0.21$$

and the subsequent undershoot is

$$\epsilon^{\frac{-3\pi}{2}} = 0.01$$

With K = 1, the response to a unit step input is

$$e_o = 1 - (1 - t)\,\epsilon^{t}$$

$$= 1 \text{ when } t = 1$$

The overshoot is

$$\epsilon^{-2} = 0.14$$

There is no undershoot. The tabulation in table 4-1 is for a value of

$$K = \frac{1}{\sqrt{2}}$$

approximately.

STANDARD CABLES

Standard cable assemblies are available for connecting external units to the SDS 925/930/9300 input/output channels and interrupt system. Table 4-2 lists model numbers and function description of these cable assemblies.

Table 4-2. Standard Cable Assemblies

Model	Function
EZ10	General purpose (no components)
EZ51	POT
EZ52	PIN
EZ61	AUX
EZ62	WRD
EZ69	External Interrupts

Each model number, to be complete, must be followed by one or two numbers separated by dashes. The first number is the length of the cable in feet; the second number is the maximum transmission delay in nanoseconds (assuming AX14 Drivers).

Permissible postscript dash numbers are listed below:

-33, -47, -75, -100, -150, -200

EZ69's are available in the following lengths:

-5, -10, -15, -22, -33, -47

Available configurations for the EZ51, EZ52, EZ61, and EZ62 are:

-5-58	-10-68	-15-68	-22-68	-	-
-5-100	-10-100	-15-100	-22-100	-33-100	-
-5-150	-10-150	-15-150	-22-150	-33-150	-47-150
-5-220	-10-220	-15-220	-22-220	-33-220	-47-220
-	-10-330	-15-330	-22-330	-33-330	-47-330

Any order for these cable assemblies which does not specify a transmission delay (second dash number) will automatically be fabricated for a delay of 150 nanoseconds.

SECTION V INTERFACE CONNECTOR PIN DESCRIPTIONS

GENERAL

This section describes in tabular form each input/output interface signal that appears on connectors attached to all input/output channels, as well as those signals that are present at the POT, PIN, and Priority Interrupt connectors. Note that all interface signals are shown within a circle or elipse - for example, (Wh). These signals are always presented as a positive level representing a logical ONE, and as a ground level representing a logical ZERO. Those interface signals shown within an elipse with a bar over the term, such as ($\overline{Zwi}$), represent a ONE when at ground level, and a ZERO when at a positive level.

TMCC INTERFACE CONNECTORS

The basic TMCC provides the following interface connectors:

Connector Positions	Designation	Function
19F, 20F, 21F	AUXW	Standard external device I/O 6-bit data and control
18F*	DISCW	Disc and drum data and control
31F, 32F	PIN	Parallel input data and control
22F, 23F, 24F	POT	Parallel output data and control
17F	MAGW	Magnetic tape data and control

With Extended Character Register:

Connector Positions	Designation	Function
10F, 11F	WRDW	Extended character register input/output data lines and control

With a second TMCC, additional interface connectors are provided.

Connector Positions	Designation	Function
14F, 15F, 16F	AUXY	Standard external device I/O 6-bit data and control
13F*	DISCY	Disc and drum data and control
12F	MAGY	Magnetic tape data and control
8F, 9F	WRDY	Extended character register input/output data lines and control

The above interface connectors are repeated for the third and fourth Time-Multiplexed Communications Channels.

*Connectors 13F (DISCW) and 18F (DISCY) may be used as AUXW and AUXY type connectors respectively if parity check need not be inhibited.

Table 5-1. TMCC W Buffer Interface Connectors (AUXW-A)

Connectors 19F, 20F, 21F
Type ZX13
Keying pins 6/26

Pin	Signal	Circuit Type	Description
1	$\overline{Zw1}$	I1	Six-bit input character lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts. $\overline{Zw6}$ becomes the least significant bit in the accumulated word.
2	$\overline{Zw2}$	I1	
3	$\overline{Zw3}$	I1	
4	$\overline{Zw4}$	I1	
5	$\overline{Zw5}$	I1	
6	$\overline{Zw6}$	I1	

Table 5-1. TMCC W Buffer Interface Connectors (AUXW-A) (Continued)

Connectors 19F, 20F, 21F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
7	$\overline{Zwp}$	I1	Odd parity bit input.
8	$\overline{Ecw}$	I3	Input or output clock supplied by the external unit. This signal must first go false (0 volts), and then true (+ volts) to initiate a character transfer. Generally $\overline{Ecw}$ = (Device Clock) $\overline{W6}$ $\overline{W5}$.
9	$\overline{Whs}$	I1	A halt signal (0 volts) supplied by the external unit to terminate an input or output process.
10	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer program to skip the next instruction in sequence.
11	Buc	O1	A signal generated for each EOM instruction, Buffer Control mode.
12	Npw	I1	A signal from external units to inhibit parity checking during input. When this line is at ground, parity is inhibited.
13	$\overline{Wes}$	I1	An error signal supplied by external units. A ground on this line indicates an error.
14	W0	O1	An halt interlock signal supplied by the TMCC. It can be used on input to denote that the input process has proceeded to process characters and on output can be combined externally with $\overline{W6}$ W5 to indicate that the last character has been processed.
15	W5	O1	A control flip-flop which detects that a precess should occur between the character register and the word assembly register. This signal can be used to interlock clock and halt operations by the external units.
16	W6	O1	A flip-flop which detects that an external clock, $\overline{Ecw}$ is present.
17	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
18	Ioc	O1	A signal generated for each EOM instruction, Input/Output mode.
19	W9	O1	Unit address register output. W9 = output $\overline{W9}$ = input
20	W10	O1	Unit address register outputs for selecting I/O devices.
21	W11	O1	
22	W12	O1	
23	W13	O1	
24	W14	O1	
25	Rw1	O1	The six-bit character register output lines. Rw6 represents the least significant bit of the character

Table 5-1. TMCC W Buffer Interface Connectors (AUXW-A) (Continued)

Connectors 19F, 20F, 21F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
26	Rw2	O1	
27	Rw3	O1	
28	Rw4	O1	
29	Rw5	O1	
30	Rw6	O1	
31	Rwp	O1	Odd parity bit generated for each output character.
32	C12	O1	Respective outputs from the C register used as address lines for the EOM and SKS operations
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	$\overline{C17}$	O1	
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-2. TMCC W Buffer Interface Connector (DISCW)

Connector 18F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
1	$\overline{Zw1}$	I1	Six-bit input character lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts. $\overline{Zw6}$ becomes the least significant bit in the accumulated word.
2	$\overline{Zw2}$	I1	
3	$\overline{Zw3}$	I1	
4	$\overline{Zw4}$	I1	

Table 5-2. TMCC W Buffer Interface Connector (DISCW) (Continued)

Connector 18F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
5	$\overline{Zw5}$	I1	
6	$\overline{Zw6}$	I1	
7	$\overline{Zwp}$	I1	Odd parity bit input.
8	$\overline{Ecw}$	I3	Input or output clock supplied by the external unit. For each input or output this signal must first go false (0 volts), and then true (+ volts) to initiate a character transfer. Generally $\overline{Ecw}$ = $\overline{(\text{Device Clock})\ \overline{W6}\ \overline{W5}}$
9	$\overline{Whs}$	I1	A halt signal (0 volts) supplied by the drum or disc unit to terminate an input or output process.
10	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction, a zero volt condition on this line will cause the computer program to skip the next instruction in sequence.
11	Buc	O1	A signal generated for each EOM instruction, Buffer Control mode.
12	Iw	O1	A signal from TMCC which indicates that the interlace is active.
13	$\overline{Wes}$	I1	An error signal supplied by drum or disc units. A ground on this line indicates an error.
14	W0	O1	An halt interlock signal supplied by the TMCC. It can be used on input to denote that the input process has proceeded to process characters and on output can be combined externally with $\overline{W6}$ W5 to indicate that the last character has been processed.
15	W5	O1	A control flip-flop which detects that a precess should occur between the character register and the word assembly register. This signal can be used to interlock clock and halt operations by the external units.
16	W6	O1	A flip-flop which detects that a drum or disc clock, $\overline{Ecw}$ is present.
17	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
18	Ioc	O1	A signal generated for each EOM instruction, Input/Output mode.
19	W9	O1	Unit address register output. W9 = output $\overline{W9}$ = input
20	W10	O1	Unit address register outputs for selecting I/O devices.
21	W11	O1	
22	W12	O1	
23	W13	O1	
24	W14	O1	

Table 5-2. TMCC W Buffer Interface Connector (DISCW) (Continued)

Connector 18F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
25	Rw1	O1	The six-bit character register output lines. Rw6 represents the least significant bit of the character.
26	Rw2	O1	
27	Rw3	O1	
28	Rw4	O1	
29	Rw5	O1	
30	Rw6	O1	
31	Rwp	O1	Odd parity bit generated for each output character.
32	C12	O1	Respective output from the C register, used as address lines for the EOM and SKS operations.
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	$\overline{C17}$	O1	
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-3. TMCC W Buffer Interface Connectors (PIN)

Connectors 31F, 32F
Type ZX13
Keying Pins 6/16

Pin	Signal	Circuit Type	Description
1	Pin	O1	A strobe signal generated each cycle during the wait phase of the PIN instruction.
2	Not Used		

Table 5-3. TMCC W Buffer Interface Connectors (PIN) (Continued)

Connectors 31F, 32F
Type ZX13
Keying Pins 6/16

Pin	Signal	Circuit Type	Description
3	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer to skip the next instruction in sequence.
4 through 7	Not Used		
8	$\overline{Rti}$	O1	A signal from the computer to external units indicating that a PIN instruction has terminated.
9 through 12	Not Used		
13	Skss	O1	A strobe signal generated for each SKS instruction.
14	Not Used		
15	$\overline{Ssc}$	I1	A response signal from external system units interrogated by an SKS instruction, System mode. A zero volt condition on this line will cause the computer to skip the instruction in sequence.
16	$\overline{Rt}$	I1	A ready signal supplied by external units (0 volts) on POT/BPO, and PIN/BPI instructions to permit data transfer.
17	Not Used		
18	$\overline{Bt}$	I1	A signal supplied by external units to the SDS 925 only to terminate BPO and BPI instructions. A ground on this line will cause the computer to halt block transfers and proceed with program.
19	$\overline{Cd24}$	I1	A parity signal used with SDS 925 BPI operations.
20	$\overline{Cd0}$	I1	The respective inputs to the C register which are used in the PIN operation. These signals are inverted before being transferred into the C register thus a logical ONE is represented by zero volts.
21	$\overline{Cd1}$	I1	
22	$\overline{Cd2}$	I1	
23	$\overline{Cd3}$	I1	
24	$\overline{Cd4}$	I1	
25	$\overline{Cd5}$	I1	
26	$\overline{Cd6}$	I1	
27	$\overline{Cd7}$	I1	
28	$\overline{Cd8}$	I1	
29	$\overline{Cd9}$	I1	
30	$\overline{Cd10}$	I1	

Table 5-3. TMCC W Buffer Interface Connectors (PIN) (Continued)

Connectors 31F, 32F
Type ZX13
Keying Pins 6/16

Pin	Signal	Circuit Type	Description
31	$\overline{Cd11}$	I1	
32	$\overline{Cd12}$	I1	
33	$\overline{Cd13}$	I1	
34	$\overline{Cd14}$	I1	
35	$\overline{Cd15}$	I1	
36	$\overline{Cd16}$	I1	
37	$\overline{Cd17}$	I1	
38	$\overline{Cd18}$	I1	
39	$\overline{Cd19}$	I1	
40	$\overline{Cd20}$	I1	
41	$\overline{Cd21}$	I1	
42	$\overline{Cd22}$	I1	
43	$\overline{Cd23}$	I1	

Table 5-4. TMCC W Buffer Interface Connectors (POT)

Connectors 22F, 23F, 24F
Type ZX13
Keying Pins 6/20

Pin	Signal	Circuit Type	Description
1	Pot1	O1	A signal from the computer indicating that the POT instruction is in a wait phase.
2	Pot2	O1	A strobe signal generated each cycle during the wait phase of the POT instruction.
3	Ioc	O1	A signal generated for each EOM instruction, Input/Output mode.
4	Buc	O1	A signal generated for each EOM instruction, Buffer Control mode.
5	Sys	O1	A signal generated for each EOM instruction, System Control mode.
6	Eom	O1	A signal generated for each EOM instruction.
7	Qq1	O1	A timing signal supplied for external use which is true from T5 through T0 of each computer cycle.
8	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
9	Pin	O1	A strobe signal generated each cycle during the wait phase of the PIN instruction.
10	$\overline{Rti}$	O1	A signal (0 volts) from the computer to external units indicating that a PIN instruction has terminated.

Table 5-4. TMCC W Buffer Interface Connectors (POT) (Continued)

Connectors 22F, 23F, 24F
Type ZX13
Keying Pins 6/20

Pin	Signal	Circuit Type	Description
11	$\overline{Bt}$	I1	A signal supplied by external units to the SDS 925 only to terminate BPO and BPI instructions. A ground on this line will cause the computer to halt block transfers and proceed with the program.
12	Qq3	O1	A timing signal supplied for external use which is true from T7 through T4 of each computer cycle. On connector 22F the signal Mtgw appears on pin 12. Its output type is I1. See pin 12, Table 5-5.
13	Skss	O1	A strobe signal generated for each SKS instruction.
14	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer to skip the next instruction in sequence.
15	$\overline{Ssc}$	I1	A response signal from external system units interrogated by an SKS instruction, System mode. A zero volt condition on this line will cause the computer to skip the instruction in sequence.
16	$\overline{Rt}$	I1	A ready signal supplied by external units (0 volts) on POT/BPO, and PIN/BPI instructions to permit data transfer.
17	St	O1	A signal from the computer derived from the manual start button on the control panel. Can be used to reset external equipment.
18	$\overline{C17}$	O1	
19	C24	O1	An output parity signal used during an SDS 925 BPO operation.
20	C0	O1	Respective outputs from C register. Used as information or address lines during the POT, SKS and EOM instructions.
21	C1	O1	
22	C2	O1	
23	C3	O1	
24	C4	O1	
25	C5	O1	
26	C6	O1	
27	C7	O1	
28	C8	O1	
29	C9	O1	
30	C10	O1	

Table 5-4. TMCC W Buffer Interface Connectors (POT) (Continued)

Connectors 22F, 23F, 24F
Type ZX13
Keying Pins 6/20

Pin	Signal	Circuit Type	Description
31	C11	O1	
32	C12	O1	
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	C17	O1	
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-5. TMCC W Buffer Interface Connector (MAGW)

Connector 17F
Type ZX13
Keying Pins 6/28

Pin	Signal	Circuit Type	Description
1	$\overline{Zw1}$	I1	Six-bit input character lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts. $\overline{Zw6}$ becomes the least significant bit in the accumulated word.
2	$\overline{Zw2}$	I1	
3	$\overline{Zw3}$	I1	
4	$\overline{Zw4}$	I1	
5	$\overline{Zw5}$	I1	
6	$\overline{Zw6}$	I1	
7	$\overline{Zwp}$	I1	Odd parity bit input.
8	$\overline{Ecw}$	I3	Input or output clock supplied by the magnetic tape unit. For each input or output this signal must first go false (0 volts), and then true (+ volts) to initiate a character transfer. Generally $\overline{Ecw}$ = $\overline{\text{(Device Clock) } \overline{W6}\ \overline{W5}}$

Table 5-5. TMCC W Buffer Interface Connector (MAGW) (Continued)

Connector 17F
Type ZX13
Keying Pins 6/28

Pin	Signal	Circuit Type	Description
9	$\overline{\text{Whs}}$	I1	A halt signal (0 volts) supplied by the magnetic tape unit to terminate an input or output process.
10	$\overline{\text{Sio}}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer program to skip the next instruction in sequence.
11	Buc	O1	A signal generated for each EOM instruction, Buffer Control mode.
12	Mtgw	I1	The magnetic tape gap signal generated by the magnetic tape unit.
13	$\overline{\text{Wes}}$	I1	An error signal supplied by the magnetic tape units. A ground on this line indicates an error.
14	W0	O1	An halt interlock signal supplied by the TMCC. It can be used on input to denote that the input process has proceeded to process characters and on output can be combined externally with the $\overline{\text{W6}}$ W5 to indicate that the last character has been processed.
15	W5	O1	A control flip-flop which detects that a precess should occur between the character register and the word assembly register. This signal can be used to interlock clock and halt operations by the external units.
16	W6	O1	A flip-flop which detects that a magnetic tape clock, $\overline{\text{Ecw}}$ is present.
17	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
18	Ioc	O1	A signal generated for each EOM instruction, Input/Output mode.
19	W9	O1	Unit address register output. W9 = output $\overline{\text{W9}}$ = input
20	W10	O1	Unit address register outputs for selecting I/O devices.
21	W11	O1	
22	W12	O1	
23	W13	O1	
24	W14	O1	
25	Rw1	O1	The six-bit character register output lines. Rw6 represents the least significant bit of the character.
26	Rw2	O1	
27	Rw3	O1	
28	Rw4	O1	
29	Rw5	O1	
30	Rw6	O1	

Table 5-5. TMCC W Buffer Interface Connector (MAGW) (Continued)

Connector 17F
Type ZX13
Keying Pins 6/28

Pin	Signal	Circuit Type	Description
31	Rwp	O1	Odd parity bit generated for each output character.
32	C12	O1	Respective outputs from the C register used as address lines for the EOM and SKS operations.
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	$\overline{C17}$	O1	
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-6. TMCC W Buffer Interface Connectors (WRDW)

Connectors 10F, 11F
Type ZX13
Keying Pins 4/24

Pin	Signal	Circuit Type	Description
1	Rw7	O1	Data outputs from extended character register Rw24 becomes least significant bit of word.
2	Rw8	O1	
3	Rw9	O1	
4	Rw10	O1	
5	Rw11	O1	
6	Rw12	O1	
7	Rw13	O1	
8	Rw14	O1	
9	Rw15	O1	

Table 5-6. TMCC W Buffer Interface Connectors (WRDW) (Continued)

Connectors 10F, 11F
Type ZX13
Keying Pins 4/24

Pin	Signal	Circuit Type	Description
10	Rw16	O1	
11	Rw17	O1	
12	Rw18	O1	
13	Rw19	O1	
14	Rw20	O1	
15	Rw21	O1	
16	Rw22	O1	
17	Rw23	O1	
18	Rw24	O1	
19	Rwp	O1	Odd parity bit for extended character.
20 through 22	Not Used		
23	$\overline{Wx12}$	I3	A signal supplied by external units that, when grounded, indicates that the character size is 12 bits.
24	$\overline{Wx24}$	I1	A signal supplied by external units that, when grounded, indicates that the character size is 24 bits.
25	$\overline{Zw7}$	I1	Data inputs to extended character register $\overline{Zw24}$ becomes least significant bit of word. The logic levels are inverted and a ONE input line is represented by zero volts.
26	$\overline{Zw8}$	I1	
27	$\overline{Zw9}$	I1	
28	$\overline{Zw10}$	I1	
29	$\overline{Zw11}$	I1	
30	$\overline{Zw12}$	I1	
31	$\overline{Zw13}$	I1	
32	$\overline{Zw14}$	I1	
33	$\overline{Zw15}$	I1	
34	$\overline{Zw16}$	I1	
35	$\overline{Zw17}$	I1	
36	$\overline{Zw18}$	I1	

Table 5-6. TMCC W Buffer Interface Connectors (WRDW) (Continued)

Connectors 10F, 11F
Type ZX13
Keying Pins 4/24

Pin	Signal	Circuit Type	Description
37	$\overline{Zw19}$	I1	
38	$\overline{Zw20}$	I1	
39	$\overline{Zw21}$	I1	
40	$\overline{Zw22}$	I1	
41	$\overline{Zw23}$	I1	
42	$\overline{Zw24}$	I1	
43	Not Used		

Table 5-7. TMCC Y Buffer Interface Connectors (AUXY-B)

Connectors 14F, 15F, 16F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
1	$\overline{Zy1}$	I1	Six-bit input character lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts. $\overline{Zy6}$ becomes the least significant bit in the accumulated word.
2	$\overline{Zy2}$	I1	
3	$\overline{Zy3}$	I1	
4	$\overline{Zy4}$	I1	
5	$\overline{Zy5}$	I1	
6	$\overline{Zy6}$	I1	
7	$\overline{Zyp}$	I1	Odd parity bit input.
8	$\overline{Ecy}$	I3	Input or output clock supplied by the external unit. For each input or output this signal must first go false (0 volts), and then true (+ volts) to initiate a character transfer. Generally $\overline{Ecy}$ = $\overline{\text{(Device Clock) } \overline{Y6}\ \overline{Y5}}$.
9	$\overline{Yhs}$	I1	A halt signal (0 volts) supplied by the external unit to terminate an input or output process.
10	$\overline{Sio}$	O1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer program to skip the next instruction in sequence.
11	Buc	O1	A signal generated for each EOM instruction, Buffer Control mode.

Table 5-7. TMCC Y Buffer Interface Connectors (AUXY-B) (Continued)

Connectors 14F, 15F, 16F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
12	Npy	I1	A signal from external devices to inhibit parity checking. When this line is at ground, parity checking is inhibited.
13	$\overline{\text{Yes}}$		An error signal supplied by external units. A ground on this line indicates an error.
14	Y0	O1	An halt interlock signal supplied by the TMCC. It can be used on input to denote that the input process has proceeded to process characters and on output can be combined externally with $\overline{Y6}$ Y5 to indicate that the last character has been processed.
15	Y5	O1	A control flip-flop which detects that a precess should occur between the character register and the word assembly register. This signal can be used to interlock clock and halt operations by the external units.
16	Y6	O1	A flip-flop which detects that an external clock, $\overline{\text{Ecy}}$ is present.
17	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
18	Ioc	O1	A signal generated for each EOM instruction, Input/Output mode.
19	Y9	O1	Unit address register output. Y9 = output $\overline{Y9}$ = input
20	Y10	O1	Unit address register outputs for selecting I/O devices.
21	Y11	O1	
22	Y12	O1	
23	Y13	O1	
24	Y14	O1	
25	Ry1	O1	The six-bit character register output lines. Ry6 represents the least significant bit of the character.
26	Ry2	O1	
27	Ry3	O1	
28	Ry4	O1	
29	Ry5	O1	
30	Ry6	O1	
31	Ryp	O1	Odd parity bit generated for each output character.
32	C12	O1	Respective outputs from the C register used as address lines for the EOM and SKS operations.
33	C13	O1	

Table 5-7. TMCC Y Buffer Interface Connectors (AUXY-B) (Continued)

Connectors 14F, 15F, 16F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	C17	O1	
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-8. TMCC Y Buffer Interface Connector (DISCY)

Connector 13F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
1	$\overline{Zy1}$	I1	Six-bit input character lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts. $\overline{Zy6}$ becomes the least significant bit in the accumulated word.
2	$\overline{Zy2}$	I1	
3	$\overline{Zy3}$	I1	
4	$\overline{Zy4}$	I1	
5	$\overline{Zy5}$	I1	
6	$\overline{Zy6}$	I1	
7	$\overline{Zyp}$	I1	Odd parity bit input.
8	$\overline{Ecy}$	I3	Input or output clock supplied by the external unit. For each input or output this signal must first go false (0 volts), and then true (+ volts) to initiate a character transfer. Generally $\overline{Ecy} = \overline{(\text{Device Clock})\ \overline{Y6}\ \overline{Y5}}$
9	$\overline{Yhs}$	I1	A halt signal (0 volts) supplied by the drum or disc unit to terminate an input or output process.

Table 5-8. TMCC Y Buffer Interface Connector (DISCY) (Continued)

Connector 13F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
10	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer processor to skip the next instruction in sequence.
11	Buc	O1	A signal generated for each EOM instruction, Buffer Control mode.
12	Iy	O1	A signal from TMCC which indicates that the interlace is active.
13	$\overline{Yes}$	I1	An error signal supplied by external units. A ground on this line indicates an error.
14	Y0	O1	An halt interlock signal supplied by the TMCC. It can be used on input to denote that the input process has proceeded to process characters and on output can be combined externally with $\overline{Y6}$ Y5 to indicate that the last character has been processed.
15	Y5	O1	A control flip-flop which detects that a precess should occur between the character register and the word assembly register. This signal can be used to interlock clock and halt operations by the external units.
16	Y6	O1	A flip-flop which detects that a drum or disc clock, $\overline{Ecy}$ is present.
17	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
18	Ioc	O1	A signal generated for each EOM instruction, Input/Output mode.
19	Y9	O1	Unit address register output. Y9 = output $\overline{Y9}$ = input
20	Y10	O1	Unit address register outputs for selecting I/O devices.
21	Y11	O1	
22	Y12	O1	
23	Y13	O1	
24	Y14	O1	
25	Ry1	O1	The six-bit character register output lines. Ry6 represents the least significant bit of the character.
26	Ry1	O1	
27	Ry3	O1	
28	Ry4	O1	
29	Ry5	O1	
30	Ry6	O1	
31	Ryp	O1	Odd parity bit. Generated for each output character.

Table 5-8. TMCC Y Buffer Interface Connector (DISCY) (Continued)

Connector 13F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
32	C12	O1	Respective outputs from the C register used as address lines for the EOM and SKS operations.
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	C17	O1	
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-9. TMCC Y Buffer Interface Connector (MAGY)

Connector 12F
Type ZX13
Keying Pins 6/28

Pin	Signal	Circuit Type	Description
1	$\overline{Zy1}$	I1	Six-bit input character lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts. $\overline{Zy6}$ becomes the least significant bit in the accumulated word.
2	$\overline{Zy2}$	I1	
3	$\overline{Zy3}$	I1	
4	$\overline{Zy4}$	I1	
5	$\overline{Zy5}$	I1	
6	$\overline{Zy6}$	I1	
7	$\overline{Zyp}$	I1	Odd parity bit input.
8	$\overline{Ecy}$	I3	Input or output clock supplied by the magnetic tape unit. For each input or output this signal must first go false (0 volts), and then true (+ volts) to initiate a character transfer. Generally $\overline{Ecy} = \overline{(\text{Device Clock})\ \overline{Y6}\ \overline{Y5}}$

Table 5-9. TMCC Y Buffer Interface Connector (MAGY) (Continued)

Connector 12F
Type ZX13
Keying Pins 6/28

Pin	Signal	Circuit Type	Description
9	$\overline{Yhs}$	I1	A halt signal (0 volts) supplied by the magnetic tape unit to terminate an input or output process.
10	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer program to skip the next instruction in sequence.
11	Buc	O1	A signal generated for each EOM instruction, Buffer Control mode.
12	Mtgy	I1	The magnetic tape gap signal generated by the magnetic tape unit.
13	$\overline{Yes}$	I1	An error signal supplied by external units. A ground on this line indicates an error.
14	Y0	O1	An halt interlock signal supplied by the TMCC. It can be used on input to denote that the input process has proceeded to process characters and on output can be combined externally with $\overline{Y6}$ Y5 to indicate that the last character has been processed.
15	Y5	O1	A control flip-flop which detects that a precess should occur between the character register and the word assembly register. This signal can be used to interlock clock and halt operations by the external unit.
16	Y6	O1	A flip-flop which detects that a magnetic tape clock, $\overline{Ecy}$ is present.
17	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
18	Ioc	O1	A signal generated for each EOM instruction, Input/Output mode.
19	Y9	O1	Unit address register output. Y9 = output $\overline{Y9}$ = input
20	Y10	O1	Unit address register outputs for selecting I/O devices.
21	Y11	O1	
22	Y12	O1	
23	Y13	O1	
24	Y14	O1	
25	Ry1	O1	The six-bit character register output lines. Ry6 represents the least significant bit of the character.
26	Ry2	O1	
27	Ry3	O1	
28	Ry4	O1	
29	Ry5	O1	
30	Ry6	O1	

Table 5-9. TMCC Y Buffer Interface Connector (MAGY) (Continued)

Connector 12F
Type ZX13
Keying Pins 6/28

Pin	Signal	Circuit Type	Description
31	Ryp	O1	Odd parity bit generated for each output character.
32	C12	O1	Respective output from the C register used as address lines for the EOM and SKS operations.
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	C17	O1	
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-10. TMCC Y Buffer Interface Connectors (WRDY)

Connectors 8F, 9F
Type ZX13
Keying Pins 4/24

Pin	Signal	Circuit Type	Description
1	Ry7	O1	Data outputs from extended character register (Ry24) becomes least significant bit of word.
2	Ry8	O1	
3	Ry9	O1	
4	Ry10	O1	
5	Ry11	O1	
6	Ry12	O1	
7	Ry13	O1	
8	Ry14	O1	
9	Ry15	O1	

Table 5-10. TMCC Y Buffer Interface Connectors (WRDY) (Continued)

Connectors 8F, 9F
Type ZX13
Keying Pins 4/24

Pin	Signal	Circuit Type	Description
10	Ry16	O1	
11	Ry17	O1	
12	Ry18	O1	
13	Ry19	O1	
14	Ry20	O1	
15	Ry21	O1	
16	Ry22	O1	
17	Ry23	O1	
18	Ry24	O1	
19	Ryp	O1	Odd parity bit for extended character.
20 through 22	Not Used		
23	$\overline{Yx12}$	I3	A signal supplied by external units that, when grounded, indicates that the character size is 12 bits.
24	$\overline{Yx24}$	I1	A signal supplied by external units that, when grounded, indicates that the character size is 24 bits.
25	$\overline{Zy7}$	I1	Data inputs to extended character register, $\overline{Zy24}$ becomes least significant bit of word. The logic levels are inverted and a ONE on an input line is represented by zero volts.
26	$\overline{Zy8}$	I1	
27	$\overline{Zy9}$	I1	
28	$\overline{Zy10}$	I1	
29	$\overline{Zy11}$	I1	
30	$\overline{Zy12}$	I1	
31	$\overline{Zy13}$	I1	
32	$\overline{Zy14}$	I1	
33	$\overline{Zy15}$	I1	
34	$\overline{Zy16}$	I1	
35	$\overline{Zy17}$	I1	
36	$\overline{Zy18}$	I1	

Table 5-10. TMCC Y Buffer Interface Connectors (WRDY) (Continued)

Connectors 8F, 9F
Type ZX13
Keying Pins 4/24

Pin	Signal	Circuit Type	Description
37	$\overline{Zy19}$	I1	
38	$\overline{Zy20}$	I1	
39	$\overline{Zy21}$	I1	
40	$\overline{Zy22}$	I1	
41	$\overline{Zy23}$	I1	
42	$\overline{Zy24}$	I1	
43	Not Used		

DACC INTERFACE CONNECTORS

Each DACC provides the following interface connectors:

Connector Positions	Designation	Function
23F, 24F, 25F	AUX	Normal speed input/output data lines (6-bit) and control
22F	DISC	Disc and drum data lines and control
21F	MAG	Magnetic tape data lines and control
3F, 4F	PIN	Parallel input data lines and control
26F, 27F	POT	Parallel output data lines and control
19F, 20F	WRD	Extended character register input/output data lines and control (normal speed)
17F, 18F	ZIN	High-speed input data lines (24) and control
15F, 16F	ZOUT	High-speed output data lines (24) and control

Table 5-11. DACC Interface Connectors (AUX)

Connectors 23F, 24F, 25F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
1	$\overline{Zz1}$	I1	Six-bit input character lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts. $\overline{Zz6}$ becomes the least significant bit in the accumulated word.
2	$\overline{Zz2}$	I1	
3	$\overline{Zz3}$	I1	
4	$\overline{Zz4}$	I1	

Table 5-11. DACC Interface Connectors (AUX) (Continued)

Connectors 23F, 24F, 25F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
5	$\overline{Zz5}$	I1	
6	$\overline{Zz6}$	I1	
7	$\overline{Zzp}$	I1	Odd parity bit input.
8	$\overline{Ecz}$	I3	Input or output clock supplied by the external unit. This signal must first go false (0 volts), and then true (+ volts) to initiate a character transfer. Generally $\overline{Ecz}$ = $\overline{\text{(Device Clock) } \overline{Z6}\ \overline{Z5}}$
9	$\overline{Zhs}$	I1	A halt signal (0 volts) supplied by the external unit to terminate an input or output process.
10	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer program to skip the next instruction in sequence.
11	Buz	O1	A signal generated for each EOD instruction, Buffer Control mode.
12	Np	I3	A signal from external units to inhibit parity checking during inputs. When this line is at ground, parity is inhibited.
13	$\overline{Zes}$	I1	An error signal supplied by external units. A ground on this line indicates an error.
14	Z0	O1	An halt interlock signal supplied by the TMCC. It can be used on input to denote that the input process has proceeded to process characters and on output can be combined externally with $\overline{Z6}$ Z5 to indicate that the last character has been processed.
15	Z5	O1	A control flip-flop which detects that a precess should occur between the character register and the word assembly register. This signal can be used to interlock clock and halt operations by the external units.
16	Z6	O1	A flip-flop that detects an external clock, $\overline{Ecz}$ is present.
17	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
18	Ioz	O1	A signal generated for each EOD instruction, Input/Output mode.
19	Z9	O1	Unit address register output. Z9 = output $\overline{Z9}$ = input
20	Z10	O1	Unit address register outputs for selecting I/O devices.
21	Z11	O1	
22	Z12	O1	
23	Z13	O1	
24	Z14	O1	

Table 5-11. DACC Interface Connectors (AUX) (Continued)

Connectors 23F, 24F, 25F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
25	Rz1	O3	The six-bit character register output lines. Rz6 represents the least significant bit of the character.
26	Rz2	O3	
27	Rz3	O3	
28	Rz4	O3	
29	Rz5	O3	
30	Rz6	O3	
31	Rzp	O3	Odd parity bit generated for each output character.
32	C12	O1	Respective outputs from the C register used as address lines for the EOD and SKS operations.
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	$\overline{C17}$	O1	External device selection signal derived from C1, C17 and C10 of the EOD instruction - true for the selected channel.
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-12. DACC Interface Connector (DISC)

Connector 22F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
1	$\overline{Zz1}$	I1	Six-bit character lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts. $\overline{Zz6}$ becomes the least significant bit in the accumulated word.
2	$\overline{Zz2}$	I1	
3	$\overline{Zz3}$	I1	

Table 5-12. DACC Interface Connector (DISC) (Continued)

Connector 22F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
4	$\overline{Zz4}$	I1	
5	$\overline{Zz5}$	I1	
6	$\overline{Zz6}$	I1	
7	$\overline{Zzp}$	I1	Odd parity bit input.
8	$\overline{Ecz}$	I3	Input or output clock supplied by the external unit. For each input or output this signal must first be false (0 volts), and then true (+ volts) to initiate a character transfer. Generally $\overline{Ecz} = \overline{(\text{Device Clock})\ \overline{Z6}\ \overline{Z5}}$
9	$\overline{Zhs}$	I1	A halt signal (0 volts) supplied by the drum or disc unit to terminate an input or output process.
10	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer program to skip the next instruction in sequence.
11	Buz	O1	A signal generated for each EOD instruction, Buffer Control mode.
12	Iz	O1	A signal from DACC which indicates that the interlace is active.
13	$\overline{Zes}$	I1	An error signal supplied by drum or disc units. A ground on this line indicates an error.
14	Z0	O1	An halt interlock signal supplied by the TMCC. It can be used on input to denote that the input process has proceeded to process characters and on output can be combined externally with $\overline{Z6}$ Z5 to indicate that the last character has been processed.
15	Z5	O1	A control flip-flop which detects that a precess should occur between the character register and the word assembly register. This signal can be used to interlock clock and halt operations by the external units.
16	Z6	O1	A flip-flop which detects that a drum or disc clock, $\overline{Ecz}$ is present.
17	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
18	Ioz	O1	A signal generated for each EOD instruction, Input/Output mode.
19	Z9	O1	Unit address register output. Z9 = output $\overline{Z9}$ = input
20	Z10	O1	Unit address register outputs for selecting I/O devices.
21	Z11	O1	
22	Z12	O1	
23	Z13	O1	
24	Z14	O1	

Table 5-12. DACC Interface Connector (DISC) (Continued)

Connector 22F
Type ZX13
Keying Pins 6/26

Pin	Signal	Circuit Type	Description
25	Rz1	O3	The six-bit character register output lines. Rz6 represents the least significant bit of the character.
26	Rz2	O3	
27	Rz3	O3	
28	Rz4	O3	
29	Rz5	O3	
30	Rz6	O3	
31	Rzp	O3	Odd parity bit generated for each output character.
32	C12	O1	Respective output from the C register used as address lines for the EOD and SKS operations.
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	$\overline{C17}$	O1	External device selection signal derived from C1, C17 and C10 of the EOD instruction - true for the selected channel.
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-13. DACC Interface Connector (MAG)

Connector 21F
Type ZX13
Keying Pins 6/28

Pin	Signal	Circuit Type	Description
1	$\overline{Zz1}$	I1	Six-bit character lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts. $\overline{Zz6}$ becomes the least significant bit in the accumulated word.
2	$\overline{Zz2}$	I1	
3	$\overline{Zz3}$	I1	

Table 5-13. DACC Interface Connector (MAG) (Continued)

Connector 21F
Type ZX13
Keying Pins 6/28

Pin	Signal	Circuit Type	Description
4	$\overline{Zz4}$	I1	
5	$\overline{Zz5}$	I1	
6	$\overline{Zz6}$	I1	
7	$\overline{Zzp}$	I1	Odd parity bit input.
8	$\overline{Ecz}$	I3	Input or output clock supplied by the magnetic tape unit. For each input or output this signal must first go false (0 volts), and then true (+ volts) to initiate a character transfer. Generally $\overline{Ecz}$ = $\overline{\text{(Device Clock) } \overline{Z6}\ \overline{Z5}}$
9	$\overline{Zhs}$	I1	A halt signal (0 volts) supplied by the magnetic tape unit to terminate an input or output process.
10	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer program to skip the next instruction in sequence.
11	Buz	O1	A signal generated for each EOD instruction, Buffer Control mode.
12	Mtg	I3	The magnetic tape gap signal generated by the magnetic tape mode.
13	$\overline{Zes}$	I1	An error signal supplied by the magnetic units. A ground on this line indicates an error.
14	Z0	O1	An halt interlock signal supplied by the TMCC. It can be used on input to denote that the input process has proceeded to process characters and on output can be combined externally with $\overline{Z6}$ Z5 to indicate that the last character has been processed.
15	Z5	O1	A control flip-flop which detects that a precess should occur between the character register and the word assembly register. This signal can be used to interlock clock and halt operations by the external units.
16	Z6	O1	A flip-flop which detects that a magnetic tape clock, $\overline{Ecz}$ is present.
17	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
18	Ioz	O1	A signal generated for each EOD instruction, Input/Output mode.
19	Z9	O1	Unit address register output. Z9 = output $\overline{Z9}$ = input
20	Z10	O1	Unit address register outputs for selecting I/O devices.
21	Z11	O1	
22	Z12	O1	

Table 5-13. DACC Interface Connector (MAG) (Continued)

Connector 21F
Type ZX13
Keying Pins 6/28

Pin	Signal	Circuit Type	Description
23	Z13	O1	
24	Z14	O1	
25	Rz1	O3	The six-bit character register output lines. (Rz6) represents the least significant bit of the character.
26	Rz2	O3	
27	Rz3	O3	
28	Rz4	O3	
29	Rz5	O3	
30	Rz6	O3	
31	Rzp	O3	Odd parity bit generated for each output character.
32	C12	O1	Respective outputs from the C register used as address lines for the EOM and SKS operations.
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	$\overline{C17}$	O1	External device selection signal derived from C1, C17 and C10 of the EOD instruction - true for the selected channel.
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-14. DACC Interface Connectors (PIN)

Connectors 3F, 4F
Type ZX13
Keying Pins 6/16

Pin	Signal	Circuit Type	Description
1	Pin	O1	A strobe signal generated each cycle during the wait phase of the PIN instruction.
2	Not Used		

Table 5-14. DACC Interface Connectors (PIN) (Continued)

Connectors 3F, 4F
Type ZX13
Keying Pins 6/16

Pin	Signal	Circuit Type	Description
3	$\overline{Sio}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer to skip the next instruction in sequence.
4 through 7	Not Used		
8	$\overline{Rti}$	O1	A signal from the computer to external units indicating that a PIN instruction has terminated.
9 through 12	Not Used		
13	Skss	O1	A strobe signal generated for each SKS instruction.
14	Not Used		
15	$\overline{Ssc}$	I1	A response signal from external system units interrogated by an SKS instruction, System mode. A zero volt condition on this line will cause the computer to skip the instruction in sequence.
16	$\overline{Rt}$	I1	A ready signal supplied by external units (0 volts) on POT/BPO, and PIN/BPI instructions to permit data transfer.
17 through 19	Not Used		
20	$\overline{Cd0}$	I1	The respective inputs to the C register which are used in the PIN operation. These signals are inverted before being transferred into the C register thus, a logical ONE is represented by zero volts.
21	$\overline{Cd1}$	I1	
22	$\overline{Cd2}$	I1	
23	$\overline{Cd3}$	I1	
24	$\overline{Cd4}$	I1	
25	$\overline{Cd5}$	I1	
26	$\overline{Cd6}$	I1	
27	$\overline{Cd7}$	I1	
28	$\overline{Cd8}$	I1	
29	$\overline{Cd9}$	I1	
30	$\overline{Cd10}$	I1	
31	$\overline{Cd11}$	I1	
32	$\overline{Cd12}$	I1	
33	$\overline{Cd13}$	I1	

Table 5-14. DACC Interface Connectors (PIN) (Continued)

Connectors 3F, 4F
Type ZX13
Keying Pins 6/16

Pin	Signal	Circuit Type	Description
34	Cd14	I1	
35	Cd15	I1	
36	Cd16	I1	
37	Cd17	I1	
38	Cd18	I1	
39	Cd19	I1	
40	Cd20	I1	
41	Cd21	I1	
42	Cd22	I1	
43	Cd23	I1	

Table 5-15. DACC Interface Connectors (POT)

Connectors 26F, 27F
Type ZX13
Keying Pins 6/20

Pin	Signal	Circuit Type	Description
1	Pot 1	O1	A signal from the computer indicating that the POT instruction is in a wait phase.
2	Pot 2	O1	A strobe signal generated each cycle during the wait phase of the POT instruction.
3	Ioz	O1	A signal generated for each EOD instruction, Input/Output mode.
4	Buz	O1	A signal generated for each EOD instruction, Buffer Control mode.
5	Syz	O1	A signal generated for each EOD instruction System Control mode.
6	Eoz	O1	A signal generated for each EOD instruction.
7	Qq1	O1	A timing signal supplied for external use which is true from T5 through T0 of each computer cycle.
8	Qq2	O1	A timing signal supplied for external use which is true from T6 through T3 of each computer cycle.
9	Pin	O1	A strobe signal generated each cycle during the wait phase of the PIN instruction.
10	$\overline{\text{Rti}}$	O1	A signal (0 volts) from the computer to external units indicating that a PIN instruction has terminated.

Table 5-15. DACC Interface Connectors (POT) (Continued)

Connectors 26F, 27F
Type ZX13
Keying Pins 6/20

Pin	Signal	Circuit Type	Description
11	Not Used		
12	Mtg	I1	Magnetic tape gap signal (26F). (Signal Qq3, T7 through T4 on 27F.)
13	Skss	O1	A strobe signal generated for each SKS instruction.
14	$\overline{\text{Sio}}$	I1	A response signal from peripheral devices interrogated by an I/O Unit Test SKS instruction. A zero volt condition on this line will cause the computer to skip the next instruction in sequence.
15	$\overline{\text{Ssc}}$	I1	A response signal from external system units interrogated by an SKS instruction, System mode. A zero volt condition on this line will cause the computer to skip the instruction in sequence.
16	$\overline{\text{Rt}}$	I1	A ready signal supplied by external units on POT and PIN instructions to release the computer from the wait phase, the computer is released when this line is at zero volts.
17	St	O1	A signal from the computer derived from the manual start button on the control panel can be used to reset external equipment.
18	$\overline{\text{C17}}$	O1	External device selection signal derived from C1, C17 and C10 of the EOD instruction - true for the selected channel.
19	Not Used		
20	C0	O1	Respective outputs from C register. Used as information or address lines during the POT, SKS, or EOD instructions.
21	C1	O1	
22	C2	O1	
23	C3	O1	
24	C4	O1	
25	C5	O1	
26	C6	O1	
27	C7	O1	
28	C8	O1	
29	C9	O1	
30	C10	O1	
31	C11	O1	
32	C12	O1	

Table 5-15. DACC Interface Connectors (POT) (Continued)

Connectors 26F, 27F
Type ZX13
Keying Pins 6/20

Pin	Signal	Circuit Type	Description
33	C13	O1	
34	C14	O1	
35	C15	O1	
36	C16	O1	
37	C17	O1	
38	C18	O1	
39	C19	O1	
40	C20	O1	
41	C21	O1	
42	C22	O1	
43	C23	O1	

Table 5-16. DACC Interface Connectors (WRD)

Connectors 19F, 20F
Type ZX13
Keying Pins 4/24

Pin	Signal	Circuit Type	Description
1	Rz7	O3	Data outputs from extended character register (normal speed). Rz24 becomes least significant bit of word.
2	Rz8	O3	
3	Rz9	O3	
4	Rz10	O3	
5	Rz11	O3	
6	Rz12	O3	
7	Rz13	O3	
8	Rz14	O3	
9	Rz15	O3	
10	Rz16	O3	
11	Rz17	O3	

Table 5-16. DACC Interface Connectors (WRD) (Continued)

Connectors 19F, 20F
Type ZX13
Keying Pins 4/24

Pin	Signal	Circuit Type	Description
12	Rz18	O3	
13	Rz19	O3	
14	Rz20	O3	
15	Rz21	O3	
16	Rz22	O3	
17	Rz23	O3	
18	Rz24	O3	
19	Rzp	O3	Odd parity bit for extended character.
20 through 21	Not Used		
22	$\overline{Zx8}$	I1	A signal supplied by external units that, when grounded, indicates that the character size is 8 bits.
23	$\overline{Zx12}$	I1	A signal supplied by external units that, when grounded, indicates that the character size is 12 bits.
24	$\overline{Zx24}$	I1	A signal supplied by external units that, when grounded, indicates that the character size is 24 bits.
25	$\overline{Zz7}$	I1	Data inputs to extended character register (normal speed). $\overline{Zz24}$ becomes least significant bit of word. The logic levels are inverted and a ONE on an input line is represented by zero volts.
26	$\overline{Zz8}$	I1	
27	$\overline{Zz9}$	I1	
28	$\overline{Zz10}$	I1	
29	$\overline{Zz11}$	I1	
30	$\overline{Zz12}$	I1	
31	$\overline{Zz13}$	I1	
32	$\overline{Zz14}$	I1	
33	$\overline{Zz15}$	I1	
34	$\overline{Zz16}$	I1	
35	$\overline{Zz17}$	I1	
36	$\overline{Zz18}$	I1	
37	$\overline{Zz19}$	I1	

Table 5-16. DACC Interface Connectors (WRD) (Continued)

Connectors 19F, 20F
Type ZX13
Keying Pins 4/24

Pin	Signal	Circuit Type	Description
38	$\overline{Zz20}$	I1	
39	$\overline{Zz21}$	I1	
40	$\overline{Zz22}$	I1	
41	$\overline{Zz23}$	I1	
42	$\overline{Zz24}$	I1	
43	Not Used		

Table 5-17. DACC Interface Connectors (ZIN)

Connectors 17F, 18F
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	GND		
2	$\overline{Zz1}$	I1	Twenty-four high-speed data input lines. The logic levels are inverted and a ONE on an input line will be represented by zero volts.
3	$\overline{Zz2}$	I1	
4	$\overline{Zz3}$	I1	
5	$\overline{Zz4}$	I1	
6	$\overline{Zz5}$	I1	
7	$\overline{Zz6}$	I1	
8	$\overline{Zz7}$	I1	
9	Shield 58		
10	$\overline{Zz8}$	I1	
11	$\overline{Zz9}$	I1	
12	$\overline{Zz10}$	I1	
13	$\overline{Zz11}$	I1	
14	$\overline{Zz12}$	I1	
15	$\overline{Zz13}$	I1	
16	$\overline{Zz14}$	I1	

Table 5-17. DACC Interface Connectors (ZIN) (Continued)

Connectors 17F, 18F
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
17	$\overline{Zz15}$	I1	
18	Shield 59		
19	$\overline{Zz16}$	I1	
20	$\overline{Zz17}$	I1	
21	$\overline{Zz18}$	I1	
22	$\overline{Zz19}$	I1	
23	$\overline{Zz20}$	I1	
24	$\overline{Zz21}$	I1	
25	$\overline{Zz22}$	I1	
26	$\overline{Zz23}$	I1	
27	Shield 60		
28	$\overline{Zz24}$	I1	
29	$\overline{Zzp}$	I1	Odd parity bit (input).
30	Np	I1	A signal from external units to inhibit parity checking during inputs. Parity checking is inhibited when this line is at ground.
31	$\overline{Ecz}$	I3	Input or output clock supplied by the external unit. For each input or output this signal must first be false (0 volts), and then true (+volts) to initiate a character transfer. Generally, $\overline{Ecz} = \overline{\text{(Device Clock) } \overline{Z5}\ \overline{Z6}}$
32	$\overline{Zx8}$	I1	An externally supplied signal specifying 8-bit character size when at 0 volts.
33	$\overline{Zx12}$	I1	An externally supplied signal specifying 12-bit character size when at 0 volts.
34	$\overline{Zx24}$	I1	An externally supplied signal specifying 24-bit character size when at 0 volts.
35	$\overline{Zft}$	I3	A signal from external units which, when at zero volt level, selects high-speed mode.
36	Shield 61		
37	Z5g	O3	Flip-flop Z5 interface signal. This flip-flop detects that a transfer of data should occur in the character register.
38	Z6g	O3	Flip-flop Z6 interface signal. This flip-flop detects that the external clock $\overline{Ecz}$ is present.
39 through 43	Not Used		

Table 5-18. DACC Interface Connectors (ZOUT)

Connectors 15F, 16F
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	GND		
2	Rz1	O3	Twenty-four high-speed data output lines.
3	Rz2	O3	
4	Rz3	O3	
5	Rz4	O3	
6	Rz5	O3	
7	Rz6	O3	
8	Rz7	O3	
9	Shield 54		
10	Rz8	O3	
11	Rz9	O3	
12	Rz10	O3	
13	Rz11	O3	
14	Rz12	O3	
15	Rz13	O3	
16	Rz14	O3	
17	Rz15	O3	
18	Shield 55		
19	Rz16	O3	
20	Rz17	O3	
21	Rz18	O3	
22	Rz19	O3	
23	Rz20	O3	
24	Rz21	O3	
25	Rz22	O3	
26	Rz23	O3	
27	Shield 56		
28	Rz24	O3	

Table 5-18. DACC Interface Connectors (ZOUT) (Continued)

Connectors 15F, 16F
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
29	Rzp	O3	Odd parity bit (output) six-bit characters only.
30	Rpe	O3	Odd parity bit (output) 8-, 12-, and 24-bit characters.
31	$\overline{Ecz}$	I3	Input or output clock supplied by external units. This signal must first go false (0 volts) then true (+ volts) to initiate a character transfer. Generally $\overline{Ecz}$ = (Device Clock) $\overline{Z5}$ $\overline{Z6}$
32	$\overline{Zx8}$	I1	An externally supplied signal specifying 8-bit character size when at ground level.
33	$\overline{Zx12}$	I1	An externally supplied signal specifying 12-bit character size when at ground level.
34	$\overline{Zx24}$	I1	An externally supplied signal specifying 24-bit character size when at ground level.
35	$\overline{Zft}$	I3	A signal from external units which, when at ground level, selects high-speed mode.
36	Shield 57		
37	Z5f	O3	Flip-flop Z5 interface signal. This flip-flop detects that a transfer of data should occur in the character register.
38	Z6f	O3	Flip-flop Z6 interface signal. This flip-flop detects that the external clock, $\overline{Ecz}$ is present.
39 through 43	Not Used		

MIC INTERFACE CONNECTOR

Each MIC provides the following interface connectors:

Connector Positions	Designation	Function
11B, 12B	MCTL	Supplies control lines for MIC input/output
31B, 32B	MIN	Input data lines (24)
21B, 22B	MOUT	Output data lines (24)

Table 5-19. MIC Interface Connectors (MCTL)

Connectors 11B, 12B
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	Not Used		
2	$\overline{Ia0}$	I1	The 15 address lines to the MIC from external units specifying the memory address to be accessed. These logic levels are inverted and a ONE is represented by zero volts.

Table 5-19. MIC Interface Connectors (MCTL) (Continued)

Connectors 11B, 12B
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
3	$\overline{Ia1}$	I1	
4	$\overline{Ia2}$	I1	
5	$\overline{Ia3}$	I1	
6	$\overline{Ia4}$	I1	
7	$\overline{Ia5}$	I1	
8	$\overline{Ia6}$	I1	
9	Shield78		
10	$\overline{Ia7}$	I1	
11	$\overline{Ia8}$	I1	
12	$\overline{Ia9}$	I1	
13	$\overline{Ia10}$	I1	
14	$\overline{Ia11}$	I1	
15	$\overline{Ia12}$	I1	
16	$\overline{Ia13}$	I1	
17	$\overline{Ia14}$	I1	
18	Shield 79		
19	$\overline{Erq}$	I1	Memory access request line from external unit. A ground level requests access.
20	$\overline{Z0}$	I1	The input/output line from external units indicating the nature of access request. A ground specifies output.
21 through 24	Not Used		
25	Zad	O3	A signal generated by the MIC and sent to external units indicating that an access request has been accepted and is being processed. Address lines must be stable when Zad is true.
26	Zdo	O3	A signal supplied by the MIC during outputs to indicate to external units that the output data lines, Moz through M23z, Mpz, are stable.
27	Shield 80		
28	Zdi	O3	A signal supplied by the MIC during inputs to indicate to the external units that the input lines, $\overline{Zio}$ through $\overline{Zi23}$, $\overline{Zip}$ are being strobed and should be stable.

Table 5-19. MIC Interface Connectors (MCTL) (Continued)

Connectors 11B, 12B
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
29	Zpe	O3	This signal is supplied by the MIC during input operations to indicate that the input word did not contain odd parity.
30 through 35	Not Used		
36	Shield 81		
37 through 43	Not Used		

Table 5-20. MIC Interface Connectors (MIN)

Connectors 31B, 32B
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	Not Used		
2	$\overline{Zi0}$	I1	Input data lines (24). The logic levels are inverted and a ONE on an input line must be represented by zero volts.
3	$\overline{Zi1}$	I1	
4	$\overline{Zi2}$	I1	
5	$\overline{Zi3}$	I1	
6	$\overline{Zi4}$	I1	
7	$\overline{Zi5}$	I1	
8	$\overline{Zi6}$	I1	
9	Shield 74		
10	$\overline{Zi7}$	I1	
11	$\overline{Zi8}$	I1	
12	$\overline{Zi9}$	I1	
13	$\overline{Zi10}$	I1	
14	$\overline{Zi11}$	I1	
15	$\overline{Zi12}$	I1	
16	$\overline{Zi13}$	I1	
17	$\overline{Zi14}$	I1	

Table 5-20. MIC Interface Connectors (MIN) (Continued)

Connectors 31B, 32B
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
18	Shield 75		
19	$\overline{Zi15}$	I1	
20	$\overline{Zi16}$	I1	
21	$\overline{Zi17}$	I1	
22	$\overline{Zi18}$	I1	
23	$\overline{Zi19}$	I1	
24	$\overline{Zi20}$	I1	
25	$\overline{Zi21}$	I1	
26	$\overline{Zi22}$	I1	
27	Shield 76		
28	$\overline{Zi23}$	I1	
29	$\overline{Zip}$	I1	Odd parity bit, input.
30 through 35	Not Used		
36	Shield 77		
37 through 43	Not Used		

Table 5-21. MIC Interface Connectors (MOUT)

Connectors 21B, 22B
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	Not Used		
2	M0z	O3	Output data lines (24).
3	M1z	O3	
4	M2z	O3	
5	M3z	O3	
6	M4z	O3	
7	M5z	O3	

Table 5-21. MIC Interface Connectors (MOUT) (Continued)

Connectors 21B, 22B
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
8	M6z	O3	
9	Shield 74		
10	M7z	O3	
11	M8z	O3	
12	M9z	O3	
13	M10z	O3	
14	M11z	O3	
15	M12z	O3	
16	M13z	O3	
17	M14z	O3	
18	Shield 75		
19	M15z	O3	
20	M16z	O3	
21	M17z	O3	
22	M18z	O3	
23	M19z	O3	
24	M20z	O3	
25	M21z	O3	
26	M22z	O3	
27	Shield 76		
28	M23z	O3	
29	Mpz	O3	
30 through 35	Not Used		
36	Shield 77		
37 through 43	Not Used		

DSC-I INTERFACE CONNECTORS

Information concerning interface connectors for the DSC-I is not available at the time of writing.

DSC-II INTERFACE CONNECTORS

The DSC-II provides the following interface connectors:

Connector Position	Designation	Function
J9D	DSC Control	W Channel Address and Control Lines
J10D	DSC Control	X Channel Address and Control Lines
J24D	DSC In	W Channel Input Data Lines
J25D	DSC In	X Channel Input Data Lines
J31C, J32C	DSC Out	W and X Channel Output Data Lines

Table 5-22. DSC-II (W) Interface Connector (DSC Control)

Connector J9D
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	GND		
2	$\overline{Wa0}$	I1	The 15 address signals supplied to the DSC-II by the external unit. The address line should be stable during the time defined by Wx. But for high-speed operations where requests are made continuously or very rapidly, Wx will remain true continuously. In this case, the address signals may be changed on the trailing edge of Wx Zad.
3	$\overline{Wa1}$	I1	
4	$\overline{Wa2}$	I1	
5	$\overline{Wa3}$	I1	
6	$\overline{Wa4}$	I1	
7	$\overline{Wa5}$	I1	
8	$\overline{Wa6}$	I1	
9	Shield 70		
10	$\overline{Wa7}$	I1	
11	$\overline{Wa8}$	I1	
12	$\overline{Wa9}$	I1	
13	$\overline{Wa10}$	I1	
14	$\overline{Wa11}$	I1	
15	$\overline{Wa12}$	I1	
16	$\overline{Wa13}$	I1	
17	$\overline{Wa14}$	I1	
18	Shield 71		

Table 5-22. DSC-II (W) Interface Connector (DSC Control) (Continued)

Connector	J9D
Type	ZX34
Keying Pins	3/47

Pin	Signal	Circuit Type	Description
19	Wsrq	I1	The request signal from external units to the DSC-II, which is enabled when the selected device wishes to input, output, or increment a word. This signal may be interlocked with Wrq, or it may be held true (low) continuously. The external unit can monitor Wx Zad signals to count completed operations. The Wsrq signal must be removed prior to Ty of the last operation or one more request will be acknowledged by the DSC-II. With interlace operations, however, the channel automatically terminates at zero count.
20	Wf3	I1	Function code signals from the external unit to the DSC-II. Refer to Table 3-15 for function codes.
21	Wf2	I1	
22	Wf1	I1	
23	Wssc	I1	A response signal generated by the selected external unit during a programmed test operation (SKS-7). The DSC-II will recognize the SKS-7 condition, however, the external unit must examine the C register outputs C12 through C23 for selection and type of test.
24	Whs	I1	A halt signal sent to the DSC-II from external units, used to cause termination of I/O or memory increment operations. The signal must be held low until halt detect flip-flop, Wh is set.
25	Zad	O1	A response signal generated in the DMC to indicate that the external unit can remove or change function code and address signal sent to the DSC-II. Zad should only be recognized when Wx is true.
26	Zdout	O1	A signal sent to external units to denote that the output data lines are stable and should be strobed. Always gate this signal with Win.
27	Shield 72		
28	Zdi	O1	A signal sent to external units to indicate that the input data lines are being strobed. This signal should only be recognized when Win is true. The occurrence of Win Zdi also indicates that the parity error signal, Zpe may be examined, or during word increment functions that the zero count signal Zdz may be strobed.
29	Zpe	O1	A parity error signal that indicates, during input operations, that the input data word did not contain an odd number of logical ONES. This line should be strobed when Win and Zdi are true.
30	Tx	O1	Timing pulse; true T4 through T1.
31	Zdz	O1	A signal sent to external units that, during the memory increment function, indicates the word count equals zero. This signal should be strobed when Win and Zdi are true.
32	Ty	O1	Timing pulse; true T0 through T8.

Table 5-22. DSC-II (W) Interface Connector (DSC Control) (Continued)

Connector J9D
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
33	Wh	O1	A halt signal generated by the DSC-II to indicate that a disconnect sequence has been completed. A halt condition exists when the halt detect flip-flop, Wh, has been set by an external halt signal, $\overline{\text{Whs}}$, or by a programmed disconnect. Flip-flop Wh may also be set when zero word count is detected on the odd interlace word if the program has not set (or has not reset) the cycle flip-flop. The signal Wh = Wh and completion of memory access.
34	Wx	O1	The signal Wx, when true, indicates to the external unit that the DSC-II has responded to a request for access to the DMC. The signal, once true, will remain true until reset by the occurrence of Zad. If the external unit is making continuous or very rapid requests, Wx will remain true.
35	Win	O1	A signal generated in the DSC-II when it has been selected by the DMC to input or output a word. Once set to the true state, Win will remain true until a request from some other DSC (or EIN) on the same DMC has been accepted.
36	Shield 73		
37	Wrq	O1	A signal sent from the DSC-II to external units, denoting that a request for operation ($\overline{\text{Wsrq}}$ low) has been detected.
38	Wioc	O1	A pseudo Ioc-type signal generated within the DSC-II. The signal occurs when an EOM 7xxxx instruction, alerting the DSC-II to the Ioc mode, is followed by a POT instruction. The timing and duration of Wioc is identical to POT2. The signal is used in conjunction with data from the POT connector to reset the subchannel's cycle flip-flop. An external device may also use Wioc to strobe the POT connector in setting various control functions.
39	Wbuc	O1	A pseudo Buc-type signal generated within the DSC-II when it is activated. An external device may use Wbuc to determine when it can strobe the computer POT connector to set initial conditions or activate the device. The signal occurs simultaneously with a POT2 computer signal.
40 through 42	Not Used		
43	$\overline{\text{Wf0}}$	I1	Not used

Table 5-23. DSC-II (X) Interface Connector

Connector J10D
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	GND		The 15 address signals supplied to the DSC-II by the external unit. The address line should be stable during the time defined by (Xx). But for high-speed operations where requests are made continuously or very rapidly, Xx will remain true continuously. In this case, the address signals may be changed on the trailing edge of (Xx) (Zad).
2	(Xa0)	I1	
3	(Xa1)	I1	
4	(Xa2)	I1	
5	(Xa3)	I1	
6	(Xa4)	I1	
7	(Xa5)	I1	
8	(Xa6)	I1	
9	Shield 70		
10	(Xa7)	I1	
11	(Xa8)	I1	
12	(Xa9)	I1	
13	(Xa10)	I1	
14	(Xa11)	I1	
15	(Xa12)	I1	
16	(Xa13)	I1	
17	(Xa14)	I1	
18	Shield 71		
19	(Xsrq)	I1	The request signal from external units to the DSC-II, which is enabled when the selected device wishes to input, output, or increment a word. This signal may be interlocked with Xrq, or it may be held true (low) continuously. The external unit can monitor (Xx) (Zad) signals to count completed operations. The (Xsrq) signal must be removed prior to (Ty) of the last operation or one more request will be acknowledged by the DSC-II. With interlace operations, however, the channel automatically terminates at zero count.
20	(Xf3)	I1	Function code signals from the external unit to the DSC-II. Refer to Table 3-15 for function codes.
21	(Xf2)	I1	
22	(Xf1)	I1	

Table 5-23. DSC-II (X) Interface Connector (DSC Control) (Continued)

Connector J10D
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
23	$\overline{Xssc}$	I1	A response signal generated by the selected external unit during a programmed test operation (SKS-7). The DSC-II will recognize the SKS-7 condition, however, the external unit must examine the C register outputs C18 through C23 for selection and C12 through C23 for selection and type of test.
24	$\overline{Xhs}$	I1	A halt signal sent to the DSC-II from external units, used to cause termination of channel operations. The signal must be held low until halt detect flip-flop, (Xh) is set.
25	Zad	O1	A response signal generated in the DMC to indicate that the external unit can remove or change function code and address signals sent to the DSC-II. (Zad) should only be recognized when (Xx) is true.
26	Zdout	O1	A signal sent to external units to denote that the output data lines are stable and should be strobed. Always gate this signal with (Xin).
27	Shield 72		
28	Zdi	O1	A signal sent to external units to indicate that the input data lines are being strobed. This signal should only be recognized when (Xin) is true. The occurrence of (Xin) (Zdi) also indicates that the parity error signal, (Zpe), may be examined or during word increment functions that the zero count signal (Zdz) may be strobed.
29	Zpe	O1	A parity error signal that indicates, during input operations, that the input data word did not contain an odd number of logical ONES. This line should be strobed when (Xin) and (Zdi) are true (high).
30	Tx	O1	Timing pulse, true T4 through T1.
31	Zdz	O1	A signal sent to external units that, during the memory increment function, indicates the word count equals zero. This signal should be strobed when (Xin) and (Zdi) are true (high).
32	Ty	O1	Timing pulse, true T0 through T8.
33	Xh	O1	A halt signal generated by the DSC-II to indicate that a disconnect sequence has been completed. A halt condition exists when the halt detect flip-flop, Xh, has been set by an external halt signal, ($\overline{Xhs}$), or by a programmed disconnect. Flip-flop Wh may also be set when zero word count is detected on the odd interlace word if the program has not set (or has not reset) the cycle flip-flop. The signal (Wh) = Wh and completion of memory access.
34	Xx	O1	The signal (Xx), when true, indicates to the external unit that the DSC-II has responded to a request for access to the DMC. The signal, once true, will remain true until reset by the occurrence of Zad. If the external unit is making continuous or very rapid requests, (Xx) will remain true.

Table 5-23. DSC-II (X) Interface Connector (DSC Control) (Continued)

Connector J10D
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
35	Xin	O1	A signal generated in the DSC-II when it has been selected by the DMC to input or output a word. Once set to the true state, Xin will remain true until a request from some other DSC (or EIN) on the same DMC has been accepted.
36	Shield 74		
37	Xrq	O1	A signal sent from the DSC-II to external units, denoting that a request for operation ($\overline{\text{Xsrq}}$ low) has been detected.
38	Xioc	O1	A pseudo Ioc-type signal generated within the DSC-II. The signal occurs when an EOM 7xxxx instruction, alerting the DSC-II to the Ioc mode, is followed by a POT instruction. The timing and duration of Xioc is identical to Pot2. The signal is used in conjunction with data from the POT connector to reset the subchannel's cycle flip-flop. An external device may also use Xioc to strobe the POT connector in setting various control functions.
39	Xbuc	O1	A pseudo Buc-type signal generated within the DSC-II when it is activated. An external device may use Wbuc to determine when it can strobe the computer POT connector to set initial conditions or activate the device. The signal occurs simultaneously with a Pot2 computer signal.
40 through 42	Not Used		
43	$\overline{\text{Xf0}}$	I1	

Table 5-24. DSC-II (W) Interface Connector (DSC In)

Connector J24D
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	Ground		
2	$\overline{\text{Wd0}}$	I1	The 24 input data lines from external units to the DSC-II. The lines are strobed when Zdi and Win are true (high).
3	$\overline{\text{Wd1}}$	I1	
4	$\overline{\text{Wd2}}$	I1	
5	$\overline{\text{Wd3}}$	I1	
6	$\overline{\text{Wd4}}$	I1	
7	$\overline{\text{Wd5}}$	I1	
8	$\overline{\text{Wd6}}$	I1	
9	Shield 80		

Table 5-24. DSC-II (W) Interface Connector (DSC In) (Continued)

Connector J24D
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
10	$\overline{Wd7}$	I1	
11	$\overline{Wd8}$	I1	
12	$\overline{Wd9}$	I1	
13	$\overline{Wd10}$	I1	
14	$\overline{Wd11}$	I1	
15	$\overline{Wd12}$	I1	
16	$\overline{Wd13}$	I1	
17	$\overline{Wd14}$	I1	
18	Shield 81		
19	$\overline{Wd15}$	I1	
20	$\overline{Wd16}$	I1	
21	$\overline{Wd17}$	I1	
22	$\overline{Wd18}$	I1	
23	$\overline{Wd19}$	I1	
24	$\overline{Wd20}$	I1	
25	$\overline{Wd21}$	I1	
26	$\overline{Wd22}$	I1	
27	Shield 82		
28	$\overline{Wd23}$	I1	
29	$\overline{Wdp}$	I1	Odd parity input line.
30 through 35	Not Used		
36	Shield 83		
37 through 43	Not Used		

Table 5-25. DSC-II (X) Interface Connector (DSC In)

Connector J25D
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	Ground		
2	$\overline{Xd0}$	I1	The 24 input data lines from external units to the DSC-II. The lines are strobed when Zdi and Xin are true (high).
3	$\overline{Xd1}$	I1	
4	$\overline{Xd2}$	I1	
5	$\overline{Xd3}$	I1	
6	$\overline{Xd4}$	I1	
7	$\overline{Xd5}$	I1	
8	$\overline{Xd6}$	I1	
9	Shield 80		
10	$\overline{Xd7}$	I1	
11	$\overline{Xd8}$	I1	
12	$\overline{Xd9}$	I1	
13	$\overline{Xd10}$	I1	
14	$\overline{Xd11}$	I1	
15	$\overline{Xd12}$	I1	
16	$\overline{Xd13}$	I1	
17	$\overline{Xd14}$	I1	
18	Shield 81		
19	$\overline{Xd15}$	I1	
20	$\overline{Xd16}$	I1	
21	$\overline{Xd17}$	I1	
22	$\overline{Xd18}$	I1	
23	$\overline{Xd19}$	I1	
24	$\overline{Xd20}$	I1	
25	$\overline{Xd21}$	I1	
26	$\overline{Xd22}$	I1	

Table 5-25. DSC-II (X) Interface Connector (DSC In) (Continued)

Connector J25D
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
27	Shield 82		
28	Xd23	I1	
29	$\overline{\text{Xdp}}$	I1	Odd parity input line.
36	Shield 83		
37 through 43	Not Used		

Table 5-26. DSC-II (W and X) Interface Connectors (DSC Out)

Connectors J31C, J32C
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
1	Ground		
2	M0s	O2	The 24 output data lines on which a word is presented, in parallel, to the external device. The output data may be strobed when Zdout and Win are true (high).
3	M1s	O2	
4	M2s	O2	
5	M3s	O2	
6	M4s	O2	
7	M5s	O2	
8	M6s	O2	
9	Shield 90		
10	M7s	O2	
11	M8s	O2	
12	M9s	O2	
13	M10s	O2	
14	M11s	O2	
15	M12s	O2	
16	M13s	O2	
17	M14s	O2	

Table 5-26. DSC-II (W and X) Interface Connectors (DSC Out) (Continued)

Connectors J31C, J32C
Type ZX34
Keying Pins 3/47

Pin	Signal	Circuit Type	Description
18	Shield 91		
19	M15s	O2	
20	M16s	O2	
21	M17s	O2	
22	M18s	O2	
23	M19s	O2	
24	M20s	O2	
25	M21s	O2	
26	M22s	O2	
27	Shield 92		
28	M23s	O2	
29	Mps	O2	Odd parity output line.
30 through 35	Not Used		
36	Shield 93		
37 through 43	Not Used		

SYSTEM PRIORITY INTERRUPT INTERFACE CONNECTORS

Each Priority Interrupt chassis provides an interface connector capable of accepting 32 interrupt lines. This connector is located in module position 44N. If the arming feature is used, the arming interrupt chassis interconnecting cable is plugged into 44N and the external interrupt input connector is plugged into 44U of the arming chassis.

Table 5-27 is typical of 28 possible Priority Interrupt connectors. Table 5-28 lists the relationship of priority lines to equivalent interrupt address locations, and gives the corresponding interrupt chassis containing the interrupts.

Table 5-27. Channel Priority Interrupt, Arming Interrupt

Connectors 44N, 44U
Type ZK54
Keying Pins 14/32

Pin	Signal	Circuit Type	Description
1 through 4	Not Used		
5	I5	I4	Thirty-two interrupt input request lines with a minimum duration of 1.75 μ seconds. The maximum duration is determined by the length of the interrupt service routine where the input line must be false before the computer resets the interrupt status flip-flops or double interruption will occur.
6	I6	I4	
7	I7	I4	
8	I8	I4	
9	I9	I4	
10	I10	I4	
11	I11	I4	
12	I12	I4	
13	I13	I4	
14	I14	I4	
15	I15	I4	
16	I16	I4	
17	I17	I4	
18	I18	I4	
19	I19	I4	
20	I20	I4	
21	I21	I4	
22	I22	I4	
23	I23	I4	
24	I24	I4	
25	I25	I4	
26	I26	I4	
27	I27	I4	
28	I28	I4	
29	I29	I4	

Table 5-27. Channel Priority Interrupt, Arming Interrupt (Continued)

Connectors 44N, 44U
Type ZK54
Keying Pins 14/32

Pin	Signal	Circuit Type	Description
30	I30	I4	
31	I31	I4	
32	I32	I4	
33	I33	I4	
34	I34	I4	
35	I35	I4	
36	I36	I4	
37 through 43	Not Used		

Table 5-28. Directory Priority Interrupt

Interrupt Address Location 925/930	Interrupt Address Location 9300	Interrupt Input Line	Interrupt Chassis	Interrupt Address Location 925/930	Interrupt Address Location 9300	Interrupt Input Line	Interrupt Chassis
200 - 237	40 - 77	I5 - I36	1	1100 - 1137	740 - 777	I453 - I484	15
240 - 277	100 - 137	I37 - I68	2	1140 - 1177	1000 - 1037	I485 - I516	16
300 - 337	140 - 177	I69 - I100	3	1200 - 1237	1040 - 1077	I517 - I548	17
340 - 377	200 - 237	I101 - I132	4	1240 - 1277	1100 - 1137	I549 - I580	18
400 - 437	240 - 277	I133 - I164	5	1300 - 1337	1140 - 1177	I581 - I612	19
444 - 477	300 - 337	I165 - I196	6	1340 - 1377	1200 - 1237	I613 - I644	20
500 - 537	340 - 377	I197 - I228	7	1400 - 1437	1240 - 1277	I645 - I676	21
540 - 577	400 - 437	I229 - I260	8	1440 - 1477	1300 - 1337	I677 - I708	22
600 - 637	440 - 477	I261 - I292	9	1500 - 1537	1340 - 1377	I709 - I740	23
640 - 677	500 - 537	I293 - I324	10	1540 - 1577	1400 - 1437	I741 - I772	24
700 - 737	540 - 577	I325 - I356	11	1600 - 1637	1440 - 1477	I773 - I804	25
740 - 777	600 - 637	I357 - I388	12	1640 - 1677	1500 - 1537	I805 - I836	26
1000 - 1037	640 - 677	I389 - I420	13	1700 - 1737	1540 - 1577	I837 - I868	27
1040 - 1077	700 - 737	I421 - I452	14	1740 - 1777	1600 - 1637	I869 - I900	28